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COMPLEMENTARY METAL-OXIDE-SILICON (CMOS)-MEMRISTOR HYBRID NANOELECTRONICS FOR ADVANCED ENCRYPTION STANDARD (AES) ENCRYPTION

SUNY POLYTECHNIC INSTITUTE COLLEGE OF NANOSCLAE
SCIENCE AND ENGINEERING

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FINAL TECHNICAL REPORT

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1. Summary

The emerging revolution of nanotechnology is expected to stimulate enormous improvements for future information technology applications. Emerging nanodevices such as carbon nanotube or graphene based transistors, tunneling devices, single electron transistors, quantum cellular automata, nanowire devices, nanojunctions, and molecular switching devices have been introduced and shown promises for future electronic applications. However, recent studies suggested that the potential benefits from completely replacing complementary metal-oxide-silicon (CMOS) devices with new types of non-silicon nanodevices may be limited. High-performance CMOS technology will remain as the primary driver for the integrated circuit (IC) industry and non-conventional nanotechnology is expected to extend and expand IC performance and function through hybridization with CMOS systems. Such hybrid-CMOS nanoelectronic systems are configured to combine the integration and scaling advantages of traditional CMOS devices with the novel functionality and performance advantages of a given class of nanodevices. This hybrid approach is engineered to enhance IC performance in the near future, while leading to module or system-level breakthroughs in the long run. Arguably, the highest profile example of this approach is the integration of high-performance, low-power memristor-based devices with conventional CMOS circuitry. Consequently, the objective of this project was to develop and demonstrate CMOS-memristor hybrid nanoelectronic circuits. Specifically, memristor nanodevices optimized for performance and reliability were developed and integrated with CMOS circuitry to establish an efficient hybrid nanoelectronic computing module for Advanced Encryption Standard (AES).

2. Introduction

The memristor is a two-terminal resistive switching memory (RRAM) nanodevice, which is recognized as the fourth fundamental electrical element in addition to resistors, capacitors, and inductors. By utilizing different resistance values to store information, memristors can function as low-power, highly-scalable device elements – critically essential properties for memory and field programmable gate array applications. More importantly, memristors have exhibited unique self-learning properties and can execute complex logic functions, which enables innovative logic, data processing, and implementation of neuromorphic systems. And, in contrast with other emerging nanoelectronic devices, memristors can utilize CMOS-compatible oxide and electrode materials, which dramatically simplifies CMOS-memristor integration. These factors underscore the promise and feasibility of large-scale CMOS-memristor hybrid nanoelectronics and point to their significant impact on future IC applications.

This project resulted in the development of novel CMOS-memristor hybrid nanoelectronics for encryption application such as the Advanced Encryption Standard (AES). AES is one of the most important encryption systems and is widely used in military and commercial systems. Based on an iterative algorithm, its hardware implementation consists of four basic operation blocks: the SubByte transformation, the ShiftRow transformation, the MixColumn transformation, and AddRoundKey. Each block requires a large amount of computational resources such as modules of XOR and AND logic functions. By using the unique complex logic function of memristors, a CMOS-memristor hybrid circuit could lead to efficient AES module implementations with high density, high speed, low power and reliable properties. Furthermore, the memristor self-learning property provides a unique opportunity to establish new encryption paradigms by changing the algorithm and building blocks that can fundamentally improve AES architecture and implementation. Thus, the development of the CMOS-memristor hybrid AES module not only enhances existing AES systems, but may establish new technology pathways for many future encryption systems.

Under this effort, the Cady Lab at CNSE (SUNY Polytechnic Institute) fabricated reliable memristors using CMOS-compatible materials, integrated memristors with CMOS devices, designed and simulated CMOS-memristor hybrid circuits, and performed reliability assessments on fabricated devices/modules. Importantly, the research leveraged a unique collaboration between AFRL/RI and CNSE to develop CMOS-memristor hybrid AES systems with advanced functionalities.

3. Methods, Assumptions and Procedures

3.1 Modeling & Simulation

Modeling and simulation were performed by co-simulation of the memristor model that was written using Verilog-A and an HSpice circuit simulator. Compact models were developed, and the memristor was modeled as a bipolar switching device. Two behavioral models were developed based on the type of electrical signal mode used to switch the device: voltage sweep mode and voltage pulsed mode. The sweep mode model of the memristive device was coded using the electrical parameters taken from electrical measurements of individual devices. The parameters were also obtained from piecewise linear approximation of its I-V curves. However, the pulsed

mode model was coded using electrical parameters taken from the literature, as the pulse mode capability of the laboratory was being set up at the time.

3.2 Fabrication

In this effort, ReRAM devices and CMOS on 300 mm wafers were built in-house at the SUNY Poly-technic Institute's Center for Semiconductor Research (CSR); however, the initial devices for materials screening were built in the laboratory of Prof. Nathaniel Cady. These initial devices were built using simple photolithographic / lift-off process. The top electrodes (TEs) for the development study were patterned using either a shadow mask or a conventional photolithography-based lift-off process. Au, Ni, Al, or Pt were deposited individually by electron beam evaporation to a final thickness of 100 nm. The resulting contacts ranged in size from 25-100 μm . For Cu_2O devices, "mesa" structures were fabricated by removing the excess Cu_2O that was not covered by the TEs. This was done through acid-based wet chemical etching of the oxide.

For the integrated CMOS / ReRAM efforts, all fabrication was performed by the CSR in CNSE's 300 mm foundry. ReRAM devices were designed and fabricated for a 300 mm wafer platform based on the IBM 65 nm 10LPe process technology. A custom, cost-effective build embeds the ReRAM devices between metal 1 (M1) and metal 2 (M2) layers. This was achieved by implementing an extra via (W-V1) below the ReRAM device. In addition, the M1 and V1 materials were changed from copper to tungsten to allow the use of front-end-of-the-line (FEOL) tools to deposit the HfO_2 serving as the active layer (metal-oxide layer) for the ReRAM device. The bottom electrode requires two consecutive damascene processes to create the dual M1/V1 stack. The first step deposits SiO_2 via chemical vapor deposition (CVD) and etches the M1 line via reactive ion etching (RIE). TiN/Ti liner is then deposited to guarantee adhesion of the CVD tungsten. A chemical-mechanical planarization (CMP) step completes M1 fabrication and leaves a flat surface for further processing. The tungsten V1 is made in the same fashion by depositing SiO_2 , etching the holes for the vias, depositing the liner and tungsten and creating a smooth surface via CMP. These steps create the inert bottom electrode on which 5.8 nm fully stoichiometric HfO_2 is deposited via Atomic Layer Deposition (ALD) followed by 6 nm PVD titanium which serves as an oxygen getter to achieve sub-stoichiometric HfO_x . The subsequent TiN deposition finishes the Optional Process (OP) layer and creates the inert top electrode. The ReRAM device is defined by a RIE etch followed by a wet HF clean creating devices with a size of $100 \times 100 \text{ nm}^2$. An n-block (SiN based material) is then deposited, serving as an etch stop during the Cu-M2/V1 RIE, followed by the standard SiO_2 insulation. A dual-damascene process creates the trenches for M2 and the holes for Cu-V1 which are then subsequently filled by PVD with a TaN/Ta liner, a copper seed layer and electroplated with copper. A final CMP step removes excess copper creating a flat surface to which one can make an electrical contact.

3.3 Device Testing

Professor Cady's lab maintains and operates a B1500A semiconductor analyzer connected to a manual probe station capable of handling 150 mm wafers or pieces of 300 mm wafers. The mainframe is equipped with four high-resolution SMU units, a capacitive measurement unit (MFCMU) and waveform generating and fast-measurement unit (WGFMU). ReRAM device characteristics were extracted by using DC-sweep as well as pulsing techniques. In both cases a one transistor one ReRAM (1T1R) setup was used to limit the current through the ReRAM during the set and forming operation to the saturation current of the transistor which was set by the transistor gate voltage. Mainly two kinds of transistors were used: **1.** an external JFET (Junction

gate field effect transistor) which was connected to the system via a discrete Keithley transistor box and 2. an integrated on-chip transistor which was implemented right underneath our integrated ReRAM. A manual probe station was used to generate preliminary results and longtime endurance measurements. DC-sweeps were preferably used to form the devices while a self-developed pulsing software in conjunction with the WGF MU enables endurance measurement up to 10^{12} cycles while recording every single cycle. Access to a semi-automatic temperature controlled 300 mm probe station equipped with the same semiconductor analyzer already operated in Cady-lab was possible at a SEMATECH owned and operated lab on the CNSE campus. This probe station was used to generate statistical data in a short amount of time as well as perform measurements at temperatures ranging from room temperature to 300C.

4. Results and Discussion

4.1 Key Accomplishments

This technical report summarizes the R&D efforts for the AFRL project “CMOS-Memristor Hybrid Nanoelectronics for AES Encryption. This research project explored CMOS-Memristor Nanotechnology Integration Research and Development for dynamically reconfigurable AES Encryption Building Blocks. The key accomplishments for this effort were:

1. *Integration of Memristor devices with SoA CMOS foundry materials and processes.*
2. *Design of hybrid CMOS-memristor test circuits and AES encryption building blocks.*
3. *Fabrication and testing of hybrid CMOS-memristor devices and circuits*

4.2 The specific tasks of the project included

Select suitable CMOS-compatible materials for memristor fabrication

- Evaluate potential memristive materials for integration with a CMOS-compatible fabrication process.
- Characterize the electrical switching properties of selected memristive materials.
- Optimize electrical properties of selected memristive materials.

Design and fabricate CMOS transistor/memristor modules for the advanced encryption standard (AES).

- Design and simulate a hybrid XOR module.
- Work with CNSE Center for Semiconductor Research to establish a process flow for integrating CMOS transistors and memristors.
- Fabricate and test a hybrid memristor/CMOS XOR module

Perform reliability studies on memristors

- Test memristors for electrical characteristic including but not limited to: Ron/Roff ratio, endurance (number of switching cycles), and switching speed.

- Explore mechanism responsible for switching behavior using data collected during reliability studies.

4.3 Materials Selection

Note: The results in this section were published as follows, during the performance of the project:

S.M. Bishop, B.D. Briggs, K.D. Leedy, S. Addepalli, N.C. Cady. A Survey of Metal Oxides and Top Electrodes for Resistive Memory Devices. (2011) *Proceedings of the Materials Research Society*, San Francisco, CA.

4.3.1 Rationale

Metal-insulator-metal (MIM) resistive switching devices are being pursued for a number of applications, including non-volatile memory and high density/low power computing. Reported resistive switching devices vary greatly in the choice of metal oxide and electrode material. Importantly, the choice of both the metal oxide and electrode material can have significant impact on device performance, their ability to switch, and the mode of switching (unipolar, bipolar, nonpolar) that results. In this study, three metal oxides (Cu_2O , HfO_x , and TiO_x) were deposited onto copper bottom electrodes (BEs). Four different top electrode (TE) materials (Ni, Au, Al, and Pt) were then fabricated on the various metal oxides to form MIM structures. Devices were then characterized electrically to determine switching performance and behavior. Our results show that the metal TE plays a large role in determining whether or not the MIM structure will switch resistively and what mode of switching (unipolar, bipolar, or non-polar) is observed.

4.3.2 Experimental

The substrates for this work consisted of a 1 μm thick electroplated copper thin film on top of Ta/TaN/ SiO_x / Si_xN_y /Si. Utilizing 300 mm wafer processing a starting substrate of SiO_2 / Si_xN_y /Si was fabricated using standard chemical vapor deposition techniques. Atop the starting substrate Cu/Ta/TaN was deposited by physical vapor deposition (PVD) as the electroplating seed, adhesion layer, and diffusion barrier, respectively. To form the Cu BE, 1 μm of electroplated Cu was deposited onto the Cu seed layer. Chemical mechanical planarization (CMP) was then used to level and polish the plated Cu, smoothing the electrode surface. This Cu film served as the BE for all devices.

Three different metal oxide films were synthesized onto the Cu BE using thermal oxidation, physical vapor deposition and atomic layer deposition (ALD). 1) TiO_x films (100 nm thick) were deposited by RF sputtering at 200 W forward power on an unheated chuck: a) in a 4.2 mTorr argon atmosphere and b) in a 4.2 mTorr argon atmosphere with an 0.1% oxygen partial pressure. These process conditions yielded a nominal deposition rate of 0.08 nm/sec. 2) HfO_x films were deposited by ALD with a chuck temperature of 250 $^\circ\text{C}$ and a chamber pressure of 0.19 torr. Process gases used were tetrakis(dimethylamido)- hafnium(IV) as the metal-organic precursor, and a 300 W RF O_2 plasma as the reactant. The target thickness of HfO_x was 50 nm, which required 603 ALD cycles, totaling 6.23 hrs of deposition time. 3) Cu_2O films were synthesized by thermal oxidation of the copper electrode at 200-400 $^\circ\text{C}$ in air at atmospheric pressure.

TEs were patterned using either a shadow mask or a conventional photolithography-based lift-off process. Au, Ni, Al, or Pt were deposited individually by electron beam evaporation to a

final thickness of 100 nm. The resulting contacts ranged in size from 25-100 μm . For Cu_2O devices, “mesa” structures were fabricated by removing the excess Cu_2O that was not covered by the TEs. This was done through acid-based wet chemical etching of the oxide. Following fabrication, electrical characterization was performed with sweep mode current-voltage (IV) measurements. R_{OFF} vs. R_{ON} values were measured in the linear portion of the IV sweep (before hitting current compliance) and approximate set/reset voltages were determined by averaging multiple (>3) on/off cycles for each device.

4.3.3 Results

TiO_x devices exhibited a wide range of electrical characteristics which were dependent upon both the TiO_x deposition method used and the TE material. In general, TiO_x deposited in an Ar-only atmosphere yielded devices with more repeatable switching behavior than TiO_x deposited in an Ar/ O_2 atmosphere. In particular, devices deposited in an Ar/ O_2 atmosphere with Al and Ni TEs exhibited diode-like behavior and could not be switched from HRS to LRS. Devices fabricated with Au and Pt TEs yielded the most consistent performance for both the Ar and Ar/ O_2 deposition conditions. These devices had similar resistive switching properties with set voltages of ~ 0.7 V, reset voltages less than -0.4 V, and $R_{\text{OFF}}/R_{\text{ON}}$ ratios of $\sim 10^6$. Interestingly, devices with Al and Au TEs exhibited unipolar switching behavior (turn-on and turn-off in the same voltage polarity) while devices with Ni and Pt TEs exhibited bipolar behavior (set and reset with opposite voltage polarity). Characteristic IV curves from TiO_x devices with Ni and Al TEs are shown in Figure 1.

Our devices behaved differently than those described in previous studies using TiO_x as the metal oxide. Kim *et al.* [1] reported both unipolar and bipolar behavior for Pt and Al TEs, while we observed only unipolar behavior for Al and only bipolar behavior for Pt. This group further showed that Ni and Al TEs yielded devices with unstable switching behavior, while we had mixed results for these electrode materials, partially dependent upon the deposition conditions of the TiO_x . Some of these differences may be due to the fact that Kim’s devices used Pt BEs, while Cu BEs were used in our devices. Since the BE material was not varied in our experiments, however, we cannot determine the overall effect it has on switching behavior.

A distinguishing feature of the TiO_x -based devices was contact bubbling and delamination (see inset in Figure 1, right side). This phenomenon is well documented by multiple research groups [2], [3] and has been suggested to be the result of oxygen released from the bulk TiO_x . Contact bubbling was most pronounced when Au was the TE. Ultimately, contact bubbling will limit the integration of TiO_x -based memory devices with CMOS systems if this issue is not addressed.

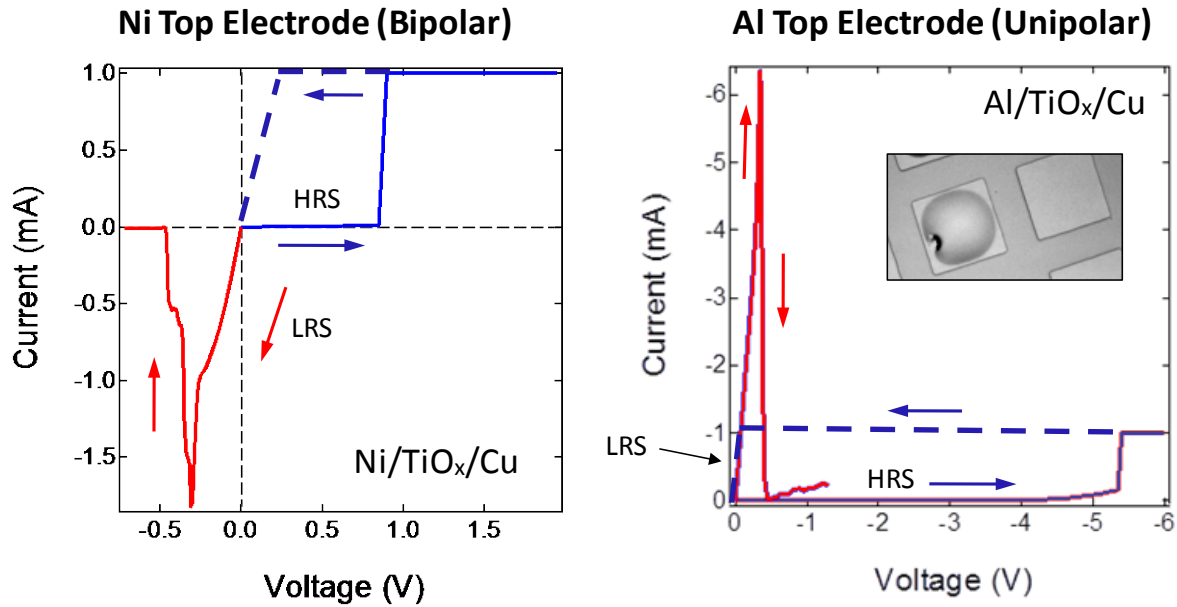


Figure 1. Current-voltage plots showing both bipolar (left) and unipolar (right) switching behavior for TiO_x devices. Bipolar behavior was observed when Ni top electrodes were used, while unipolar behavior was observed for devices with Al top electrodes. Top electrode bubbling and delamination (right, inset) was observed for all TiO_x devices, regardless of top electrode material.

HfO_x-based devices exhibited non-polar switching behavior independent of the TEs and without the need for a forming voltage. Non-polar behavior was exhibited by the ability to switch in both a unipolar and bipolar manner, regardless of TE material. In addition, set voltages less than ± 1 V and reset voltages on the order of ± 500 mV were observed with average R_{OFF}/R_{ON} ratios of 10^8 . Examples of IV switching behavior for HfO_x-based devices are shown in Figure 2, below. Although this figure shows data from two different devices (one with a Ni TE and one with an Al TE) both unipolar and bipolar switching were observed for both of these TE materials.

Unipolar, bipolar and non-polar switching behavior have all been observed for HfO_x-based devices [4], [5]. Similar to the TiO_x results (above), this could potentially be due to the Cu BE used in this study. Cu may well play a role in the switching behavior that is observed for some of these devices and other work by our group has shown that Cu may diffuse to the upper surface of the HfO_x during the deposition process [6]. This could have significant influence on the switching behavior of these devices.

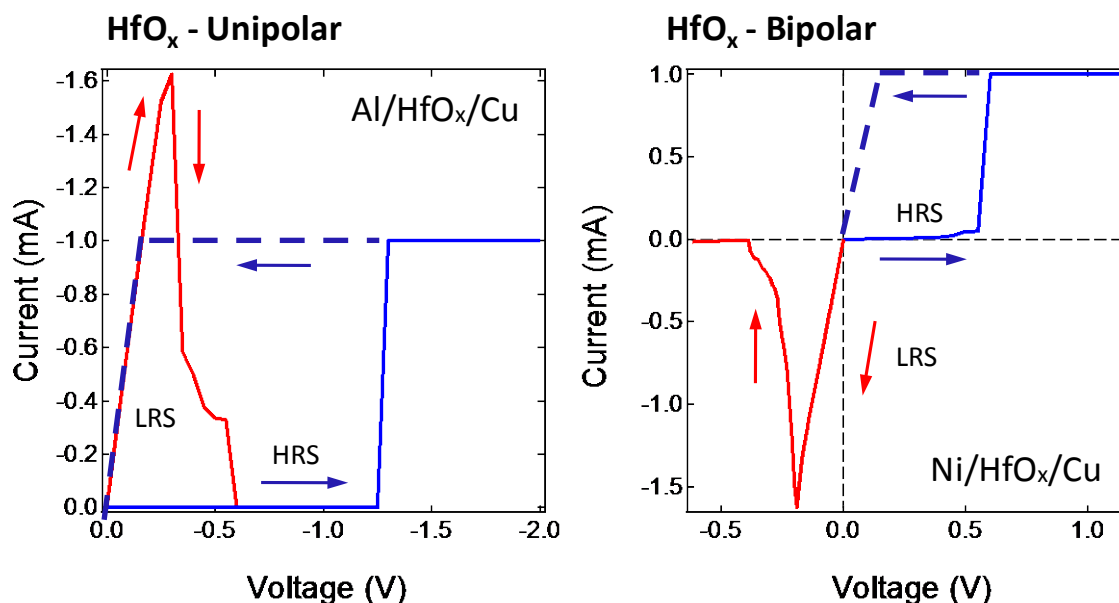


Figure 2. Current-voltage plots showing both unipolar (left) and bipolar (right) switching behavior for HfO_x devices. Switching behavior for HfO_x devices was independent of electrode material.

Cu₂O device behavior was strongly dependent upon TE material, and these devices did not demonstrate resistive switching behavior with either Au or Ni TEs. Further, only “mesa” devices exhibited consistent switching behavior. Devices that contained a continuous thermal oxide layer showed diode behavior independent of the top electrode. Mesa devices fabricated with Pt and Al TEs exhibited only bipolar switching behavior and repeated attempts at unipolar switching were unsuccessful. Current-voltage characterization indicated that the Cu₂O devices with Al TEs switch more consistently (at similar set and reset voltages) than those fabricated with Pt TEs. For the Cu₂O devices with an Al TE, set voltages ranged from 1.5-2.5 V, and reset voltages were less than -1 V. The R_{OFF}/R_{ON} ratio for these devices ranged from 10³-10⁴. An example IV curve is shown in Figure 3 (below) for a Cu₂O device with an Al TE.

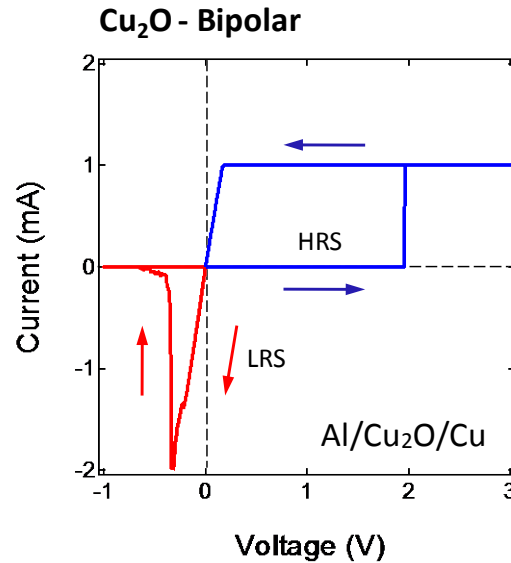


Figure 3. Current-voltage plot showing bipolar resistive switching behavior of Cu_2O based devices with Al top electrodes and Cu bottom electrodes.

4.3.4 Summary

In summary, devices with three types of metal oxides (Cu_2O , HfO_x , and TiO_x) demonstrated resistive switching characteristics which were highly dependent upon the type of material used for the TE. The results from this study are compiled in Table 1, below. This work shows that TE selection is an important factor for determining the resistive switching properties of MIM devices, and that this factor alone can determine switching polarity. Notably, not all TE / metal oxide combinations yielded switchable devices. Our work did not examine the role of the BE, since all devices tested used Cu BEs. The major result of these experiments was that due to ease of fabrication and excellent device performance, HfO_x was selected as the primary dielectric material for use in subsequent memristor device fabrication.

4.4 Simulation, Design and Fabrication

Note: Portions of this section are an excerpt from the PhD dissertation of Dr. Benjamin Briggs and Jihan Capulong, graduate students who worked on this project. The dissertations are entitled “Investigation of HfO_x/Cu Resistive Memory for Advanced Encryption Applications” and “Oxide Defect Engineering Methods for Valence Change (VCM) Resistive Random Access Memories”, respectively.

4.4.1 Rationale

The advanced encryption standard (AES) hardware implementation is primarily comprised of XOR logic. Our goal was to implement hybrid CMOS / ReRAM circuit alternatives for raw performance, power, or density improvements. A proof of concept was needed to determine the fabrication and performance feasibility of these new hybrid designs. Two circuit modules were

selected, one based on reconfigurable XOR logic in which the resistive memory allowed the CMOS XOR gates to be reconfigured dynamically, and the other was a NOR gate based on the hybrid CMOL-Icell design in which the resistive memory elements play a part in logic gate.

4.4.2 Simulation

SPICE

Simulation Program for Integrated Circuits Emphasis (SPICE) is a general-purpose analog circuit simulator that was developed at the Electronics Research Laboratory of the University of California, Berkeley [6]. In 1975, SPICE simulation became the industry standard for verification of integrated circuit (IC) and board-level designs to check circuit integrity and predict the circuit behavior at transistor level before manufacturing. Doing so allows designers to evaluate the designs without physically building them, which in turn saves time and money.

SPICE became a popular simulation tool because it can perform several types of circuit analyses and also contained device models that were necessary to design integrated circuits at the time. At the same time, SPICE is robust and fast enough for the task [7]. For example, the BIAS simulation program can only simulate the bipolar junction transistor's (BJT) operating point [8]. Another program called SLIC is only capable of small-signal analyses [9]. Some types of circuit analyses that SPICE can do are the following:

- DC analysis – determines the DC operating point or quiescent point of a circuit.
- AC small-signal analysis – computes the AC output variables as a function of frequency.
- Transient analysis – computes the transient output variables as a function of time over a time interval.
- Noise analysis – computes the device-generated noise for a given circuit.
- Distortion analysis – computes the steady-state harmonic and inter-modulation products.
- Fourier analysis – calculates and plots the frequency spectrum of a circuit.
- Monte Carlo analysis – a statistical analysis that calculates the circuit response when device model parameters are randomly varied between the tolerance limits of a given distribution.

SPICE relies on models for the behavior of various circuit elements from simple models such as that for resistors, capacitors, and inductors, to the more complex models such as that for bipolar junction transistor (BJT) or MOSFET. Built-in models are available, and the user can specify values for pertinent model parameters. For example, the model for the BJT in SPICE is based on the integral-charge model of Gummel and Poon [10], but when the parameters are unspecified, the Eber-Moll model is used [11]. Secondary and non-linear effects are also implemented on the models such as charge-storage effects, ohmic resistances, and current-dependent output conductance. Several models are included for MOSFET devices: MOS1 is described by the square-law, MOS2 [12] and MOS3 [12] for the analytical and empirical models respectively, MOS6 is a simple analytic model with good accuracy in the short-channel region [13], and the Berkley Short-channel IGFET Model (BSIM) family of models that has become standard MOSFET models in the industry [14]–[16]. Other circuit components are also available in SPICE such as transmission lines, operational amplifiers, switches, and independent and dependent voltage and current sources. SPICE analyses can be done at different temperatures with the default temperature of 300 K.

To perform circuit simulation in SPICE, a *netlist* is provided as input into the program. The netlist describes the connections of the circuit elements together (topology) and their values, the user-defined parameters needed in the device models. It also contains *control statements* which specify the type of analysis to be performed, and *output statements* which specify the output signals that will be plotted. The netlist is translated in SPICE into nonlinear differential algebraic equations, which are solved by implicit integration methods [7], Newton's method [17], and sparse matrix techniques [18]. The netlist structure is shown in Figure 4.

```
Title Statement
Element Statements
.
.
Control Statements
Output Statements
.END <CR>
```

Figure 4. SPICE netlist structure

SPICE was initially made available as an open source program. This made it widely distributed and used, both in academia and industry. This also allowed other free and commercially available versions of SPICE to be developed. Some popular versions are PSPICE, Spectre, Eldo, and HSPICE. This work used HSPICE to perform the circuit simulations.

Verilog-A

Verilog-A is a hardware description language (HDL) for analog circuit and systems. It is one of the two HDLs in the Verilog family of languages, which includes Verilog-HDL used for describing digital components [19]. A hardware description language differs from traditional programming languages (C/C++, Java, PERL, etc.) for it is used to describe hardware, while programming languages are used to describe algorithms. The two main applications of HDL are simulation and synthesis. In simulation, a stimulus is applied to an executable model that was written in HDL in order to predict its response. This allows one to understand how a complex system will behave before actual implementation which saves time and cost. The model, however, has to be able to describe a wide variety of behaviors in order to be effective in simulation with various stimuli. Synthesis is the process of actually implementing the hardware. The HDL is used to describe the hardware at an abstract level using component models that do not have physical implementation, and then synthesis is the act of creating a new description of the same system with equivalent input and output behaviors using components that have actual physical implementations. Synthesis appears like a black-box, wherein a design described by the HDL goes in, and what comes out is a gate- or component-level netlist that can be physically implemented.

Verilog-HDL was introduced in 1984 and became the standard in 1995 for the specification and design of digital systems [20]. The main advantage of using Verilog-HDL is that it allows specifying of digital systems at multiple levels of abstraction, from behavioral to structural. Verilog-A was then introduced for analog systems in order to take advantage of the same feature. Previously, analog simulation was mainly performed using the SPICE circuit simulator or some derivative of it. Despite the effectiveness and accuracy of SPICE as a simulation tool, SPICE is limited to structural level of representation and is also limited to the use of primitive components

such as resistors, transistors, and capacitors. In the past, this limitation was circumvented using programs such as Matlab that allow description of electronic and non-electronic systems in higher levels of abstraction based upon numeric computation and data analysis. Albeit useful, these programs do not tie into other tools such as SPICE and Verilog, which makes design and simulation very complicated. Verilog-A also allows mathematical description of a system, but with the advantage of being interfaced readily to SPICE. Verilog-A was designed to be compatible with, and an extension of SPICE for both low and high levels of abstraction (e.g., circuit level). Verilog-A borrowed its syntax from Verilog-HDL, while semantics was derived from SPICE such as the supported types of design and analyses.

In Verilog-A, the behavioral descriptions are mathematical mappings of the input signals into the system to the output signals out of the system. These can be written in terms of large-signal or time-domain behavioral descriptions. A mathematical expression is assigned to a signal which can be linear/non-linear, algebraic and/or differential functions of the input signal. The *contribution operator*, $<+$, is used to map or assign an expression to a signal. The mapping takes the form:

$$output_signal < + f(input_signal) \quad (1)$$

In Verilog-A, a system (an individual device or a circuit) can be represented as a black box with two nodes, p and n , having an associated potential difference between them, $V(p,n)$, and a current flow, $I(p,n)$ (Figure 5). The positive node (+) indicates the node with a higher potential, and also where the current flow enters the system.

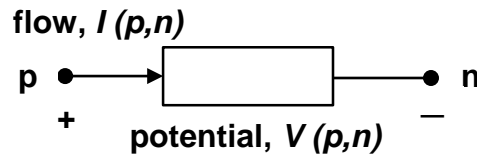


Figure 5. Associated potential (voltage) and flow (current) in an electrical system with nodes, p and n .

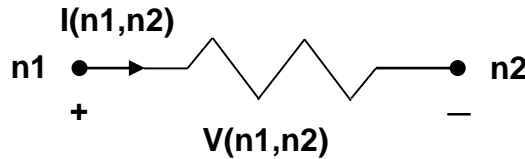


Figure 6. Resistor model and reference directions in Verilog-A.

To illustrate how to model a system using Verilog-A, consider the simple example of resistor in Figure 6. The behavior of the resistor is modeled by its voltage and current relationship described by Ohm's Law,

$$I(n1,n2) = V(n1,n2)/R, \quad (2)$$

where R is the resistance value of the resistor. The behavior of a resistor with an $R = 1$ ohm can be written in Verilog-A as,

```

module resistor (n1, n2);
    inout n1, n2;
    electrical n1, n2;

    parameter real R = 1.0;

    analog
        I(n1, n2) <+ V(n1, n2) / R;

Endmodule

```

Figure 7. Verilog-A model of a linear resistor.

Modeling and simulation were performed by co-simulation of the ReRAM model, written using Verilog-A, using the HSPICE circuit simulator. Compact, behavioral models were developed for the bipolar type of ReRAM based on the type of electrical signal mode used to switch the device during testing: either voltage sweep mode or voltage pulse mode. In a voltage sweep mode test, the device is biased with an increasing voltage signal across its terminals. The current response is then plotted versus the applied voltage, also known as I-V curve. Parametric information about the device could be obtained from this plot, such as switching threshold voltages (V_{set} and V_{reset}), resistance levels (R_{on} and R_{off}), and reset switching current level. The voltage pulse mode test is useful to obtain transient response of a system such as switching speed and response times. A voltage pulse signal is applied across the terminal that is usually sufficient to switch the device. The response of a device in pulse mode is also very important to obtain since CMOS circuits are operated in pulse mode.

Sweep mode model

The behavioral model for sweep mode was taken from electrical measurements of individual HfO_x -based ReRAM devices using the Agilent B1500A semiconductor parametric analyzer. Switching and device parameters were taken from the I-V curves with the following definitions (Figure 8):

- Threshold voltages
 - V_{set} – defined as the voltage level at which the current signal abruptly increased.
 - V_{reset} – defined as the voltage at the peak current.
 - V_{off} – defined as the voltage when R_{off} is reached.
 - V_{on} – defined as the voltage when the current compliance or R_{on} is reached.
- Resistance states
 - R_{on} – the slope of the line fitted between V_{reset} and V_{set} in the forward sweep
 - R_{off} – the slope of the line fitted between V_{reset} and V_{set} in the reverse sweep

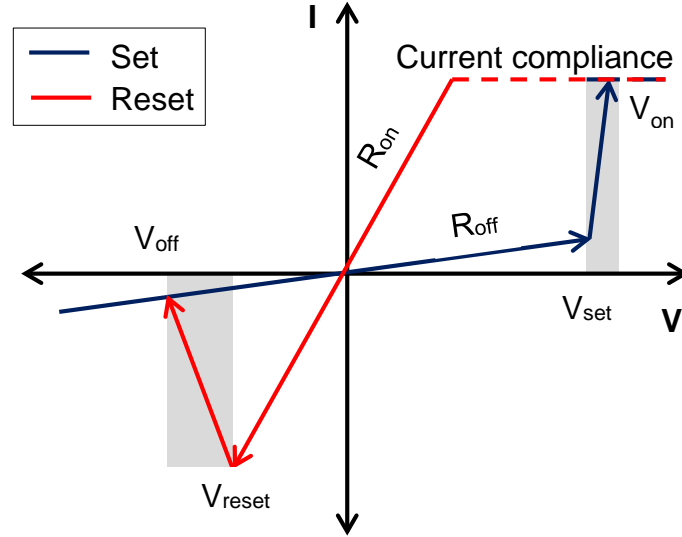


Figure 8. I-V curve of a bipolar ReRAM showing the parameters defined in the sweep mode model. The arrows indicate the direction of the sweep. The gray areas highlight the transition regions during switching (set and reset processes).

An excerpt of the Verilog-A code of the bipolar ReRAM device model is shown in Figure 9. The set process occurs when the voltage is positively swept, while a reset process occurs in the negative direction. The model also breaks the I-V curve up into piecewise lines similar to those shown in Figure 8. In the model, the device ultimately switches between two resistance states, R_{on} or R_{off} , when the switching threshold values, V_{on} or V_{off} , are reached. For the set process, the device will take on the resistance value of R_{on} when the voltage threshold, V_{on} , is reached. For the reset process, the resistance value will be R_{off} when V_{off} is reached. The mapping equation of the ReRAM behavior before the device reaches the set/reset threshold voltage and after the device has switched to R_{on} or R_{off} follows the Ohm's law,

$$I(n1,n2) < + V(n1,n2)/res, \quad (3)$$

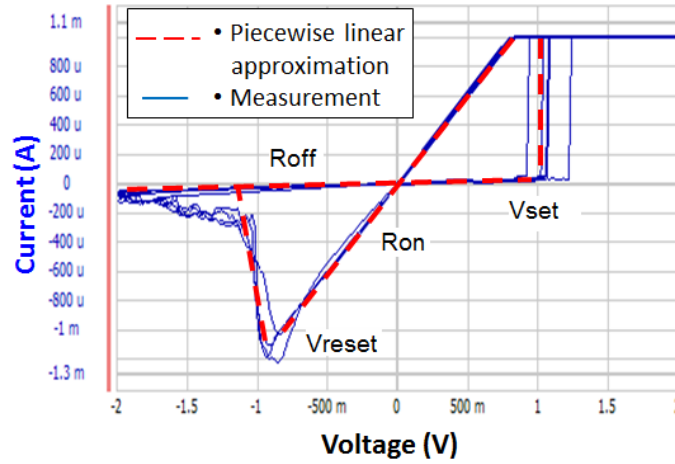
```

initial res = Roff
analog begin
  V=V(n1,n2);
  //Set process
  if (res==Roff) begin
    if (V>=Von) begin                                //Set process completed
      res=Ron;
      I(n1,n2) <+ V(n1,n2)/res;
    end
    else begin
      if (V<=Vset)                                //Before Vset or Vreset reached
        I(n1,n2) <+ V(n1,n2)/res;
      else begin                                    //Transition region
        m = (Von/Ron - Vset/Roff)/(Von-Vset);
        I(n1,n2) <+ m*(V(n1,n2)-Vset)+Vset/res;
      end
    end
  end
  //Reset process
  else begin
    if ((V<=Vreset)&&(V>Voff)) begin //Transition region
      m = (Voff/Roff - Vreset/Ron)/(Voff-Vreset);
      I(n1,n2) <+ m*(V(n1,n2)-Vreset) + Vreset/res;
    end
    else begin
      if (V<=Voff)                                //Reset process done
        res = Roff;
        I(n1,n2) <+ V(n1,n2)/res;
      end
    end
  end

```

Figure 9. Excerpt of the Verilog-A code that models the sweep-mode behavior of the bipolar ReRAM device that is initially in HRS.

(a)



(b)

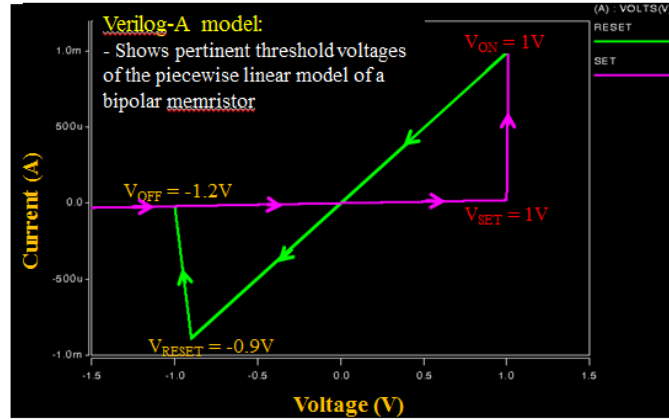


Figure 10. shows that the resulting I-V curve after simulation replicates that of the linearly approximated I-V curve from measurements, with the correct threshold voltages that were encoded into the model. This shows that the model, albeit simple, is effective in representing the behavior of the ReRAM in sweep mode.

where, $res = R_{on} \text{ or } R_{off}$. The model also takes into account the transition regions, the gray areas in Figure 9. Excerpt of the Verilog-A code that models the sweep-mode behavior of the bipolar ReRAM device that is initially in HRS., during switching events. A switching event can be simply modeled as a discontinuity or abrupt switching between R_{on} and R_{off} . Even though this is allowed in Verilog-A, there is a risk of non-convergence in circuit simulation. Modeling the transition region reduces this risk. It also takes into account the multi-level switching in ReRAM. For example, multi-level resistance can be achieved with R_{on} by varying the value of the current compliance [21], [22], or by doing consecutive sweeps or pulses [23], [24].

To demonstrate the sweep mode modeling, a HfO_x -based bipolar ReRAM device with TiN and W electrodes from Sematech was electrically tested (Figure 10 a). The details of the fabrication are described in [25]. At least 10 repeat measurements were taken from the device, and the mean of the necessary model parameters were calculated. The mean values of the model parameters are as follows: $V_{set} = 1 \text{ V}$, $V_{reset} = -0.9 \text{ V}$, $V_{off} = -1.2 \text{ V}$, $R_{on} = 1 \text{ k}\Omega$ and $R_{off} = 500 \text{ k}\Omega$. These parameters

were then encoded into the Verilog-A sweep mode model. The model was then validated by simulating it in HSPICE. The netlist for this circuit described an individual ReRAM device that is connected with a sweeping voltage source.

Pulse Mode Model

A different approach was taken for pulse mode modeling. Electrical measurements were unavailable in pulse mode, due to the limitations of our electrical testing setup. Due to the lack of empirical data, it was necessary to appeal to memristor device theory described in Chapter 1 to develop the model. Memristance relates charge to flux (Equation 1.8). It is then natural to surmise, that the switching event may be triggered by satisfying an electric flux threshold, as opposed to meeting a threshold voltage. In such a model, a switching event threshold for flux, the time integral of the applied voltage, was set and the history of applied voltage and duration was compared to this threshold (Equation 1.6-1.7). Once met, the model sets the device. In a similar manner, though using the opposite voltage polarity, the device would reset.

The sweep mode model operated upon a threshold voltage switch mechanism, since the applied signal was supplied with the intent to fully set or reset the device. Under an arbitrary pulse scheme, this method could not readily be applied. Thus, based upon the flux threshold switching hypothesis, a low voltage pulse of long duration, a high voltage pulse of short duration, and a medium voltage pulse applied repeatedly were all capable of transitioning the ReRAM device to the low resistance state provided the flux threshold was attained. In order for the simulated device to be able to achieve intermediate states, a piecewise linear model was employed as a proof-of-concept, where resistance of the ReRAM would change in a linear fashion (Figure 11). Such an approach was supported by the few pulse-operation papers available in the literature [26], [27]. As the resistance approached its maximum value, the overall change upon device behavior was minimal; whereas, for a device approaching the minimum value, the decrease in resistance was very gradual before reaching the lower limit abruptly. Such behavior is generally consistent with a linear resistance change.

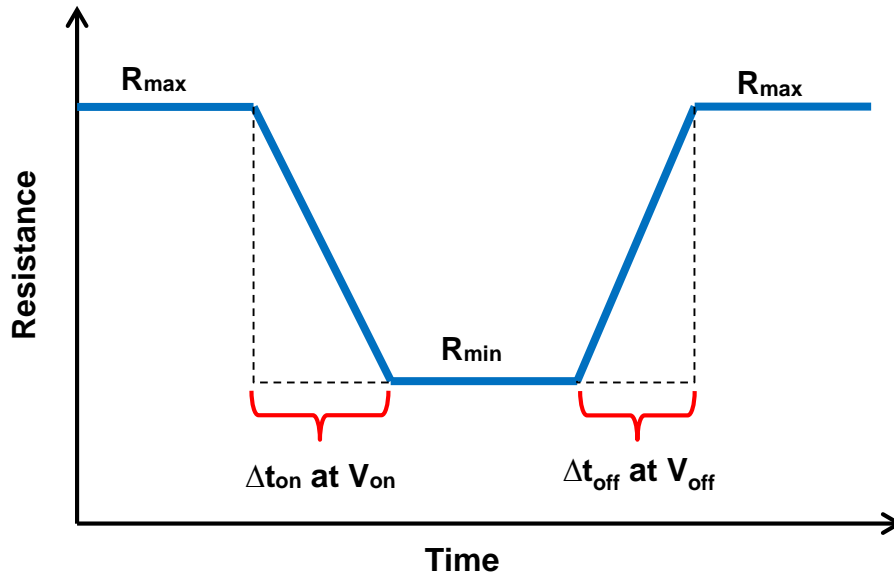


Figure 11. Piecewise linear approximation of the resistance when applied with set or reset pulse.

The parameters needed in the pulse mode model are the following:

- R_{\min} – the minimum achievable low resistance state.
- R_{\max} – the maximum achievable high resistance state.
- V_{on} – set threshold voltage needed to achieve R_{\min} .
- V_{off} – reset threshold voltage needed to achieve R_{\max} .
- Δt_{on} – the amount of time required to set the device to R_{\min} when biased at V_{on} .
- Δt_{off} – the amount of time required to reset the device to R_{\max} when biased at V_{off} .

In the end, the operational parameters of this model included the minimum and maximum resistance values and the threshold flux value for both set and reset operations. The mapping equation between current and voltage for the pulse mode model also uses the Ohm's law (2). The maximum or minimum resistances, R_{\max} or R_{\min} respectively, is used when the required amount of flux, φ_{on} and φ_{off} , which are determined by,

$$\varphi_{\text{on}} = \Delta t_{\text{on}} * V_{\text{on}} \quad (4)$$

$$\varphi_{\text{off}} = \Delta t_{\text{off}} * V_{\text{off}} \quad (5)$$

The transition between R_{\min} and R_{\max} is described by the following equations,

$$R_{i+1} = R_i - (R_{\max} - R_{\min}) \left(\frac{\varphi_{i+1}}{\varphi_{\text{on}}} \right) \text{ for set, and} \quad (6)$$

$$R_{i+1} = R_i + (R_{\max} - R_{\min}) \left(\frac{\varphi_{i+1}}{\varphi_{\text{on}}} \right) \text{ for reset} \quad (7)$$

As with the sweep mode model, the pulse mode model was translated into Verilog-A to run in HSPICE. Two simulations were performed. The first simulation was to show the effect of providing pulses that would fully switch the device from the HRS (R_{\max}) to LRS (R_{\min}). The second simulation was to show the effect of providing an arbitrary set of pulses that would enable partial switching. Figure 12 and Figure 13 are comprised of three graphs each in which the first graph shows the voltage pulse applied, the resulting current response is shown in the second graph, and the change in resistance over time is shown in the third. Figure 12 shows the switching response of the device when provided with set and reset pulses and also read pulses to check the resistance state after switching. As mentioned, these pulses should be sufficient to completely switch the device from HRS to LRS. As can be seen for the set function, the resistance abruptly decreases as it reaches the threshold and then gradually changes to the LRS at the end of the pulse. Reset is triggered as the negative threshold voltage is reached. A linear change of resistance is then seen as it goes from LRS to HRS. The read pulse provided after each switching did not trigger further resistance changes and thus showed the resistance state after the switching process. Figure 13 then shows that response of the device when biased with a shorter, 50 ns pulse, instead of the 110 ns pulse in Figure 12. As the resistance plot at the bottom of Figure 13 shows, the resistance starts off in HRS and once triggered with the voltage pulse, the device begins to decrease in resistance towards the LRS. The short pulse is only able to reduce the resistance to an intermediate resistance level between HRS and LRS, $R_{\text{intermediate}}$. By providing another set of pulses which completes the required flux, the final resistance, R_{\min} , was achieved. Proceeding from LRS to HRS afterwards shows a similar trend: several pulses are needed to completely switch the device from LRS to HRS.

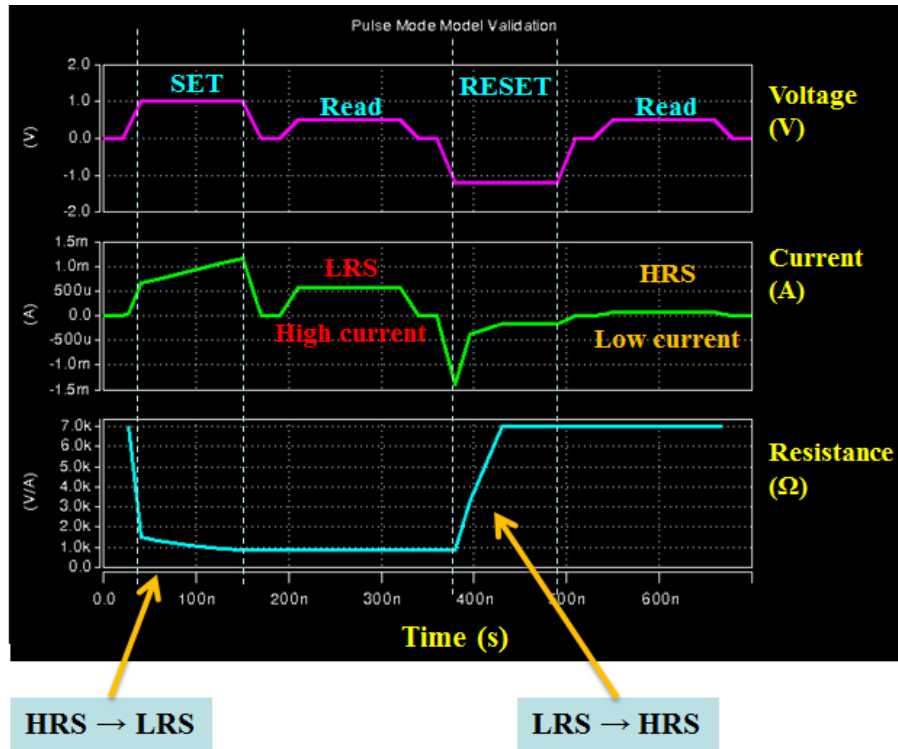


Figure 12. Pulse mode model demonstration of full cycle ReRAM switching using Verilog-A and HSPICE, where $V_{SET} = 1V$, $V_{RESET} = -1.2V$, $t_{SET} = t_{RESET} = 110ns$, $R_{SET} = 3k\Omega$, and $R_{RESET} = 7k\Omega$.

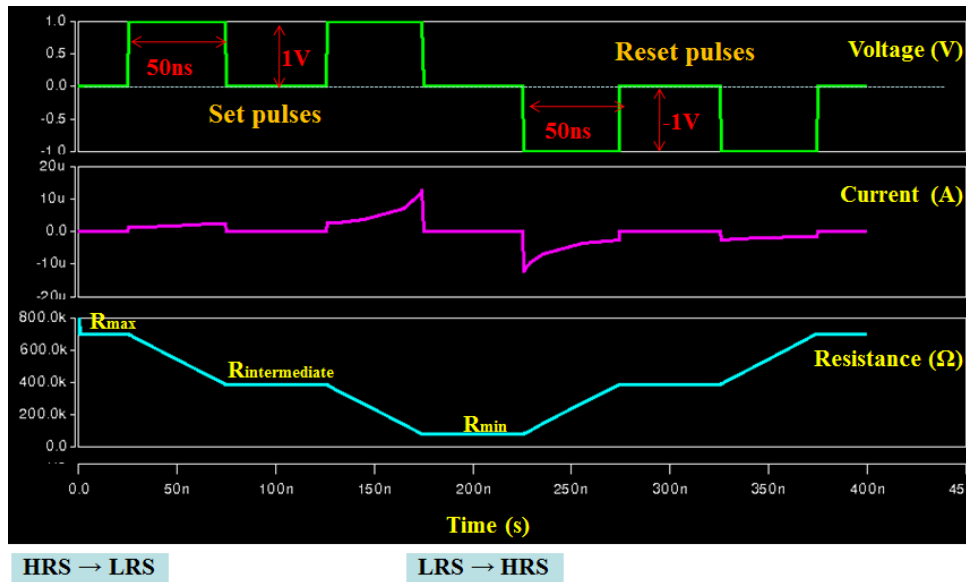


Figure 13. Pulse mode model demonstration of switching via multiple pulses (in this case two pulses) to elicit a full set or reset operation.

4.4.3 Chip Design / Layout

The first circuit to be implemented was in application of the MixColumns module of AES. The MixColumns module is 100% XOR in nature, so our circuit is of course an XOR gate. Figure

14 depicts a single cell of the XOR array in this cell design. The fully arrayed design for a MixColumns operation can be seen in Z. Abid et al. (Abid, Z., Alma, A., Member, S., Barua, M. & Wang, W. Efficient CMOL Gate Designs for Cryptography Applications. *IEEE Trans. Nanotechnol.* **8**, 315–321 (2009)). The resistive memory elements and their connections are represented in the electrical diagram of Figure 14 by the nanowires and junction resistor elements. Three total resistive memory elements are used in this circuit, not for logic purposes but to allow the central XOR gate to be connected to others in the array using reconfigurable interconnect topologies. This proof of concept circuit includes just one XOR gate connected to three resistive memory devices, as in Figure 14. The XOR gate is constructed differently than a typical CMOS implementation; it uses three inverters (at two transistors each). Two of the inverters are included to boost the logic (voltage) levels due to any drop from the interconnects or the resistive memory element. Lastly there are two transmission gates (nmos and pmos connected in parallel) that perform the final XOR function, for another four transistors. Transmission gates operate as simple switches, with the application of V_{DD} to the control gate(s) current is allowed to flow across the device. A total of ten transistors are needed for this single XOR cell, compared to that of a conventional CMOS gate of 3-10 transistors (there are several XOR designs with different performance tradeoffs that influence the number of transistors needed in a single gate).

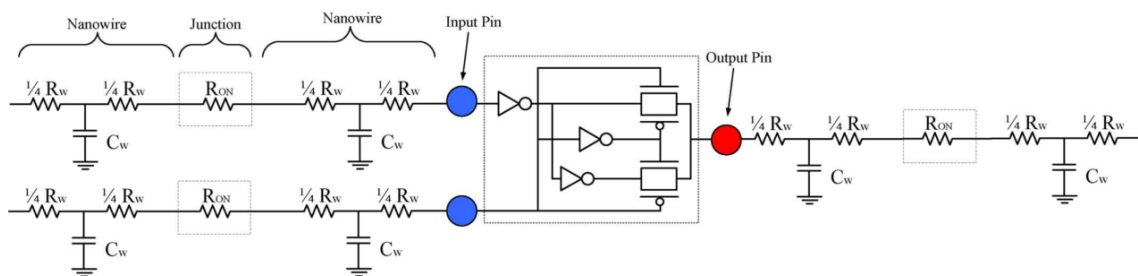


Figure 14. Hybrid ReRAM/CMOS XOR cell.

The second circuit module to be designed is a CMOL NOR gate. CMOL is the combination of CMOS and any nano-device, it is a blanket term for hybrid circuitry in which the nano-devices provide a density, performance, and/or power improvement to a particular circuit. The CMOL NOR gate is depicted in schematic form in Figure 14 (left). Resistive memory elements are depicted by resistors in the figure labeled R_{ON} . Inputs to the NOR gate are supplied to resistive memory elements and are wired in parallel as inputs A, B to “n” allowing for a “n” input NOR gate to be constructed. The downstream resistive memory connections are wired into the input of a CMOS inverter for the NOT function. A pass transistor is located as R_{PASS} to create the high impedance voltage divider necessary to supply sufficient logic level voltage to the CMOS inverter, and to allow for current controlled programming of the resistive memory elements. Diode elements are also needed on each input line to protect from current sneak paths back into other inputs, similar to the passive cross bar sneak path problem. These diodes can be external, fabricated with the resistive memory as a 1D1R configuration, or part of the resistive memories behavior if it has strong nonlinear switching behaviour. The comparison of the CMOL NOR gate can be seen in Figure 15 (right) to its purely CMOS counterpart. For a two input NOR gate the CMOL circuit has a roughly 2X reduction in area compared to the CMOS circuit. This is due to the loss of one transistor, reduction in interconnect length, and the ability to place the diode and resistive memory directly above the transistors. For multiple input NOR gates the CMOL design yields an increased area reduction proportional to the number of inputs.

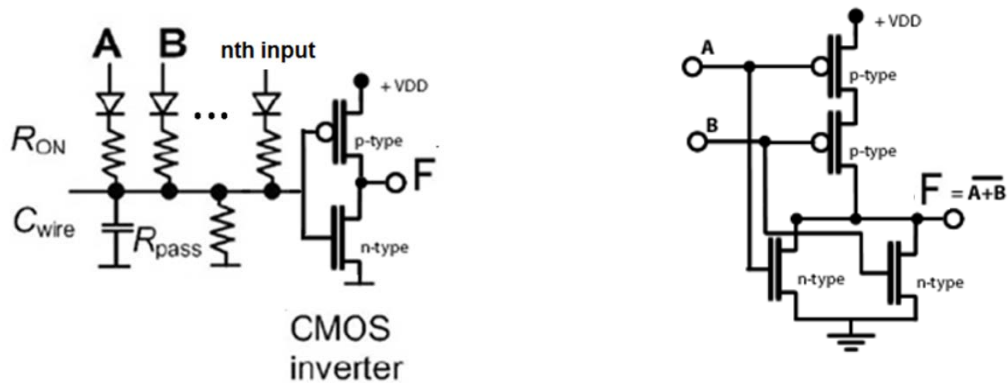


Figure 15. CMOL NOR layout (left). CMOS NOR layout (right)

The IBM 10LPe 65 nm low power CMOS process design kit (PDK) was used to design the two CMOL circuit modules as well as several other test circuits (described below in Table 1). Features of 10LPe process are an operating voltage V_{DD} of 1.2 V for thin oxide (2.6 nm) and 2.5 V for thick oxide (5.7 nm) devices, twin well technology on a p type substrate, shallow trench isolation for reduced device coupling, stress engineered channels for enhanced mobility, minimum drawn gate length of 60 nm, low resistance self-aligned nickel silicide for n+ and p+ poly silicon and substrate contacts, copper contact studs to connect substrate and poly silicon gates to first metal, planarized passivation and interlevel low-k dielectrics with copper interconnects for low resistance/capacitance. Cadence Virtuoso 6.0 was used in conjunction with the 10LPe PDK. Virtuoso is a full layout / design rule check (DRC) and simulation platform. The IBM PDK inputs directly into the Virtuoso layout software and allows for common circuit elements to be generated with variable geometries and design features.

Using Cadence Virtuoso and the IBM 10LPe PDK, transistor instances were generated and the required number of nmos and pmos were placed in the design for a particular circuit. The transistor dimensions were dictated by current requirements of the resistive memory components. A range of drive currents from 2 mA to device min (363 μ A) were chosen for maximum compatibility with the yet unknown resistive memory characteristics. All gate lengths were drawn at minimum critical dimension of 60 nm to minimize device area and maximize drive currents. Gate widths were adjusted accordingly for desired drive current. For instance a 2 mA nFET with a drive current spec. of 605 μ A/ μ m would have a gate width of 3.3 μ m. Gate widths longer than 1 μ m were converted into a multi gate / finger parallel FET's to minimize interconnect length and create more compact designs. The multi gate FET is essentially a geometric trick to create higher

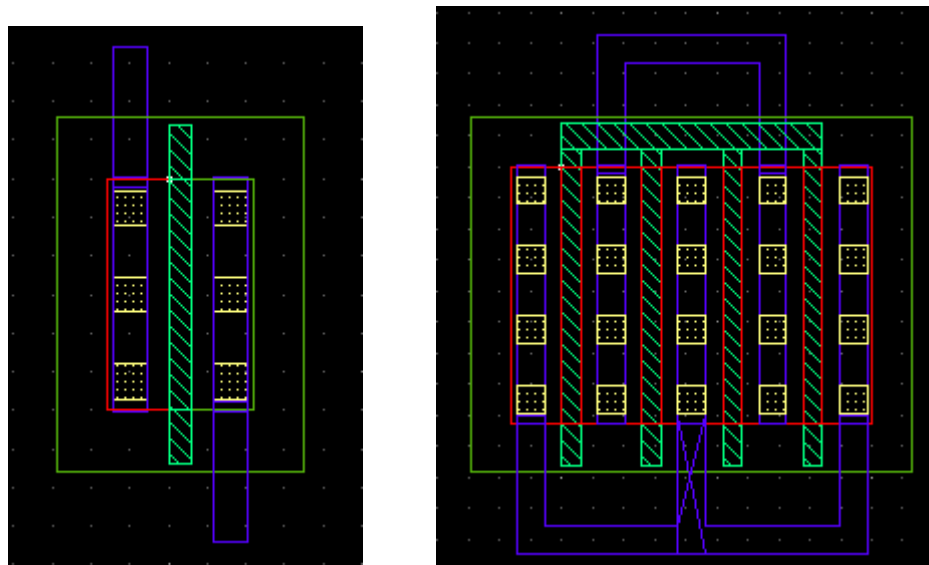


Figure 16. 363 μA NFET (left). 2 mA NFET with multi gate layout (right).

drive current transistors without unrealistically wide designs. The source and drains of several lower drive current transistors are tied together with a common gate, in a parallel arrangement. In layout, this can be accomplished by sharing the source region of the first parallel transistor with the source of the next transistor and so on. This creates a reduction in area due to the shared source drain regions. Figure 16 (left) depicts the general layout of a single NFET with a 60 nm gate (green/PC mask level) length and a design minimum gate width corresponding to a drive current of 363 μA . Contact studs (yellow/CA mask level) and Metal 1 (Blue/M1 mask level) are drawn at 90 nm, and process modification was used to shrink the source / drain contact studs (CA) to ~65 nm. The multi gate design is depicted in Figure 16 (right) with an effective gate width of 3.3 μm but a drawn single gate width of just 0.8 μm . The 10LPe process also has three FET variants, a regular threshold voltage reg- V_T device, a low- V_T , and a high voltage (3.3V) I/O device dgh- V_T .

Each of the circuits were replicated with the three different transistor types and three different drive currents or gate widths for a total of nine redundant and varying designs for each circuit module. Example of a reg- V_T CMOL XOR circuit is shown in Figure 7. The five pFETs are all arranged in the same n well at the top of the design, likewise the nFETs are located in the same p well at the bottom. The pFET's have a double gate design, which was used to boost their drive current to match that of the nFET's. pFET's have roughly half the drive current per gate width than nFET's due to the lower mobility of holes in Si ($-315 \mu\text{A}/\mu\text{m}$). Three interconnect levels PC, M1, and M2 are used to wire the FET's together in accordance with the CMOL XOR circuit diagram of Figure 7.

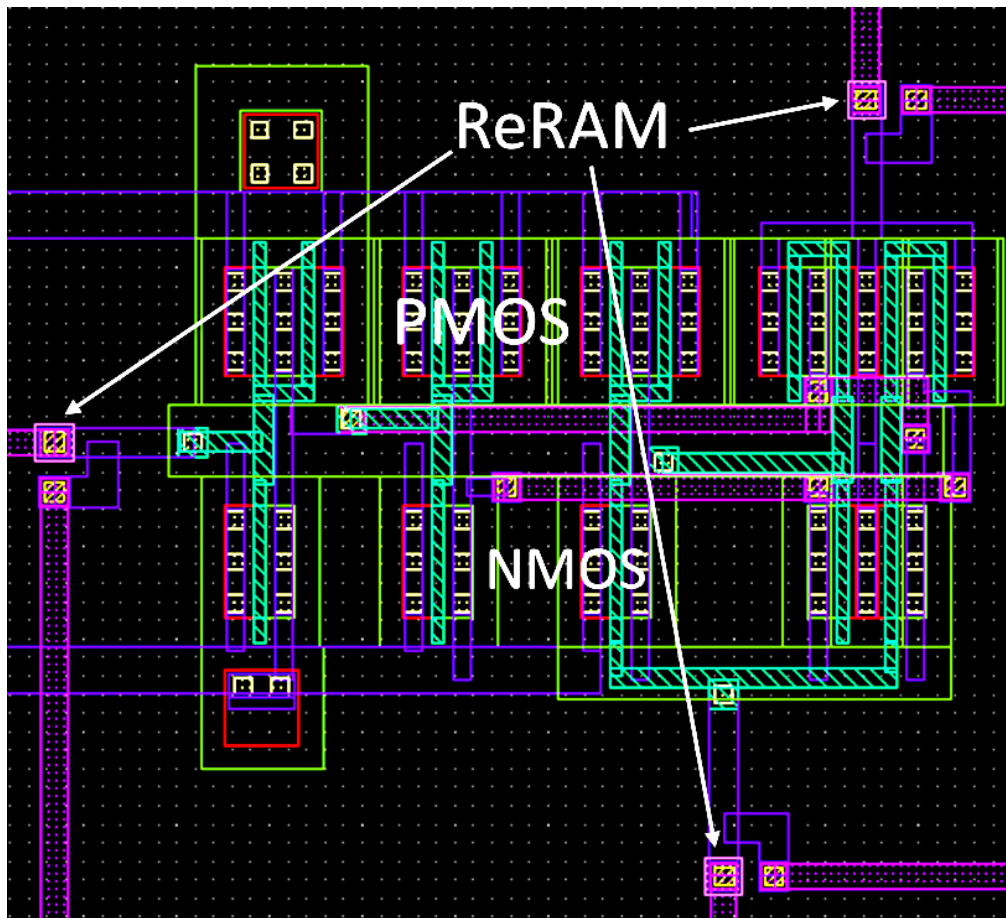


Figure 17. Layout of hybrid XOR logic cell.

The three resistive memory elements, two for the input pins and one for the output are shown on the periphery of Figure 17. Each resistive memory element also has a separate interconnect to the BE allowing the resistive memory and the XOR circuit to operate and be tested independently from each other. The separate connection will aid in bench testing and diagnostics during preliminary fabrication.

The CMOL NOR circuit is laid out in a similar fashion with $\text{reg-}V_T$ 363 μA drive current as seen in Figure 18. Again the pFET and nFET regions were laid out in separate blocks to minimize interconnect leakage and create compact designs.

The individual resistive memory layout is of importance in these designs, as it will have strong implications for the fabrication process. The 10LPe PDK does not contain design rules or instances for a resistive memory device as they are not part of any commercial process or product, so an improvised design was created. A kelvin design was adopted to remove the effects of contact resistance during electrical measurements. The design is that of a single junction cross point device as seen in Figure 19. In this figure, M1 serves as the bottom electrode and runs horizontally in blue, out to two separate contact pads for the kelvin geometry. The OP level in pink defines the boundary of the resistive memory oxide or active layer. The V1 layer in orange will be used to create the top electrical contact to the resistive memory, followed by M2 in purple carrying the TE signal out to the kelvin arrangement pads.

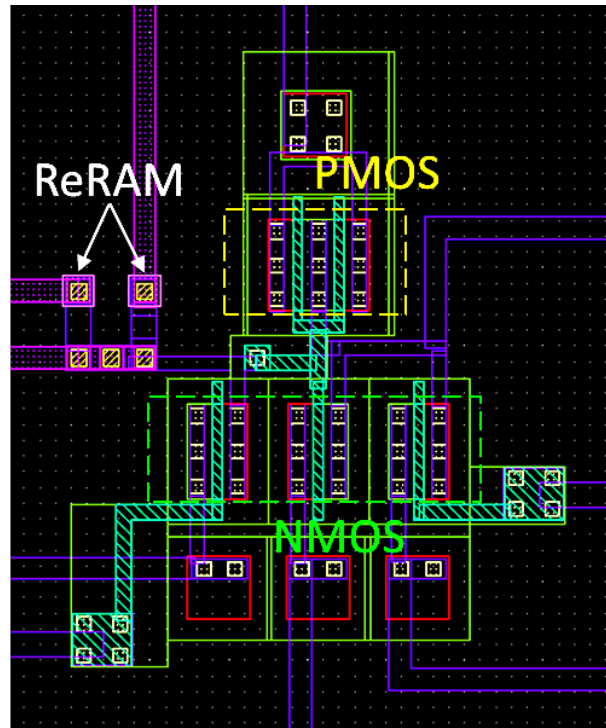


Figure 18. CMOL circuit layout.

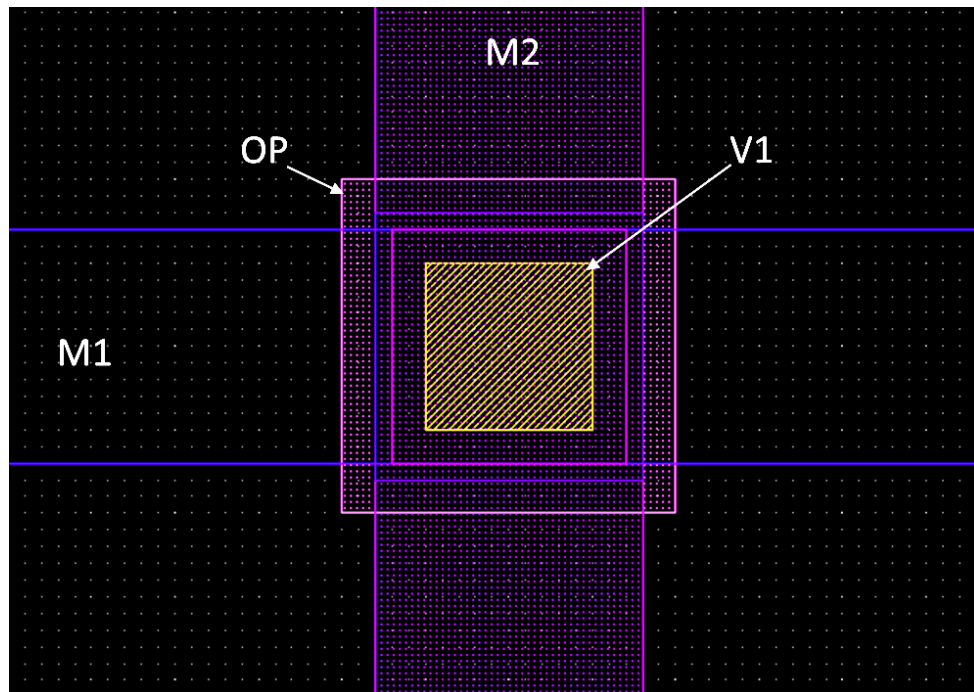


Figure 19. Single ReRAM layout.

Along with the individual Kelvin resistive memory structures, there are several 1T1R designs (not shown) with varying transistor types, just as the CMOL designs. There are also large passive crossbar arrays ranging from 12x12 to 128x128 (16 Kb) to test for array scaling properties. There

is also a 5x5 three-layer design to test the 3D stacking capability of the device structures, a requirement for high density MLC type resistive memory. A list of all circuits and device structures with geometry details can be found in Table 1.

The full chip design incorporates all of the resistive memory development structures in redundant rows along with CMOL circuits in double redundant blocks. Figure 20 shows an overview of the full chip design. The resistive memory development occupies roughly 33% of the chip and the redundant double blocks of AES circuits the other 66% of the area. The mask set for this particular design is part of larger multi project wafer (MPW). MPW's allow several research groups to combine designs onto one mask set to save costs. Our particular MPW was given the code name of Raptor. Our chip area on Raptor measures 6.6 x 2.9 mm. Within that area devices are arranged vertically with contact pads in a 1 x 25 arrangement, allowing for in line electrical test to be performed with IBM standard probe cards. The last point to mention is the inclusion of SIMS pads (pads for secondary ion mass spectrometry analysis) on the far right of the Raptor chip. These large 200 x 200 μm pads are drawn at M1/OP/V1/M2 so that a SIMS depth profile can be obtained after fabrication to confirm composition and interfaces of respective layers.

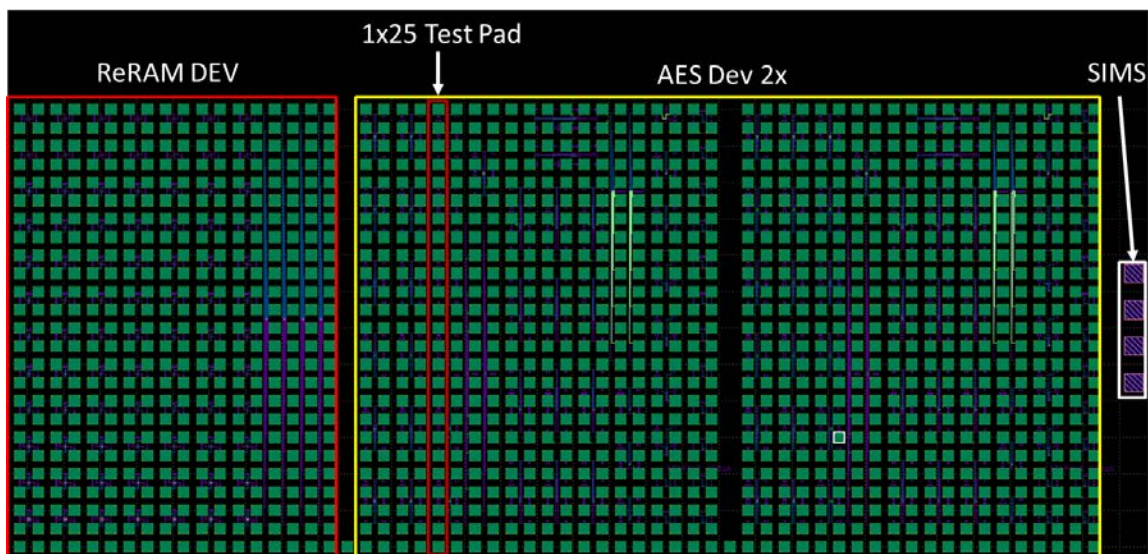


Figure 20. Raptor Chip 1 layout.

Table 1. Documentation of all Raptor test structures.

Circuit	Qty	CMOS Type	NMOS	PMOS	RRAM	Pads /struct	Total Pads	Device Geometry
XOR	3	Reg-Vt	5	5	3	8	24	2mA W=3.3um, 1mA W=1.653um, 0.363mA W=0.6um
XOR	3	Low-Vt	5	5	3	8	24	2mA W=2.74um, 1mA W=1.37um, 0.438mA W=0.6um
XOR	1	DG-HVt	5	5	3	8	8	2mA W=3.306um (3.3V IO FETs)
CMOL NOR	3	Reg-Vt	3	1	2	10	30	2mA W=3.3um, 1mA W=1.653um, 0.363mA W=0.6um
CMOL NOR	3	Low-Vt	3	1	2	10	30	2mA W=2.74um, 1mA W=1.37um, 0.438mA W=0.6um
CMOL NOR	1	DG-HVt	3	1	2	10	10	2mA W=3.306um (3.3V IO FETs)
12x12 Xbar	2	none	0	0	144	24	48	100nm V1 spec
5x5x5 3layer Xbar	1	none	0	0	125	15	15	reuse OP for 2nd RRAM layer
2x2 Xbar	1	none	0	0	8	4	4	100nm V1 spec
128x128 Xbar	1	none	0	0	16384	256	256	100nm V1 spec
1T2R FPGA	1	Reg-Vt	1	0	2	5	15	W=0.6um, 3.3um
1R	12	none	0	0	1	4	48	100nm(V1), 150nm(V1), 200nm(V1), 300nm(V1), 500nm(V1), 750nm(V1), 1um(V1), 2um(V1), 5um(V1), 10um(V1)
1T1R	3	Reg-Vt	1	0	1	4	12	2mA W=3.3um, 1mA W=1.653um, 0.363mA W=0.6um
1T1R	3	Low-Vt	1	0	1	4	12	2mA W=2.74um, 1mA W=1.37um, 0.438mA W=0.6um
1T1R	1	DG-HVt	1	0	1	4	4	2mA W=3.306um (3.3V IO FETs)
2X2 1T1R	2	Low-Vt	4	0	4	8	16	2mA W=2.74um, 1mA W=1.37um

4.4.4 Chip Fabrication Development:

To start the fabrication development of the Raptor mask set and its hybrid circuitry we first started with the back end of the line (BEOL) portion of the design, which encompasses only the resistive memory. This was done for efficiency. Since the IBM 10LPe process was adopted for the design we could use the PDK and design flow. The process was copied and moved to the CNSE 300 mm fabrication line. This meant there would be a large ramp up time before the CMOS portion of the process became stable and tuned. Since the management and optimization of a new CMOS flow is a multi-person effort (and was assigned to process engineers at CNSE) we chose to focus on the BEOL process unique to our design and let the CNSE engineering team perform the CMOS process transfer from IBM in parallel.

The fabrication of a resistive memory device on an industry compatible 300 mm process is a serious undertaking and is currently still in development. Since resistive memory is a simple MIM structure, it is rather easy to fabricate. Since we are working in the constraints of the 10LPe PDK, however, we do not have a mask level to implement the resistive memory layer. We needed a mask layer that is known as a blocking layer, which allows drawn features to appear as resist printed on wafer for the purposes of a subtractive etch process. We also needed the mask layer to have a minimum CD to allow for small devices on the order of 100 nm, and lastly the layer had to be not required elsewhere. The OP mask layer was selected as it met all of the design criteria and was intended for silicide resistors which were not part of our circuits. Figure 21 shows a schematic cross-section of a Cu/HfO₂/TiN resistive memory device (right) with back side contact (left) of the proposed fabrication flow. Using M1 as a BE simplifies fabrication and provides the device material system desired.

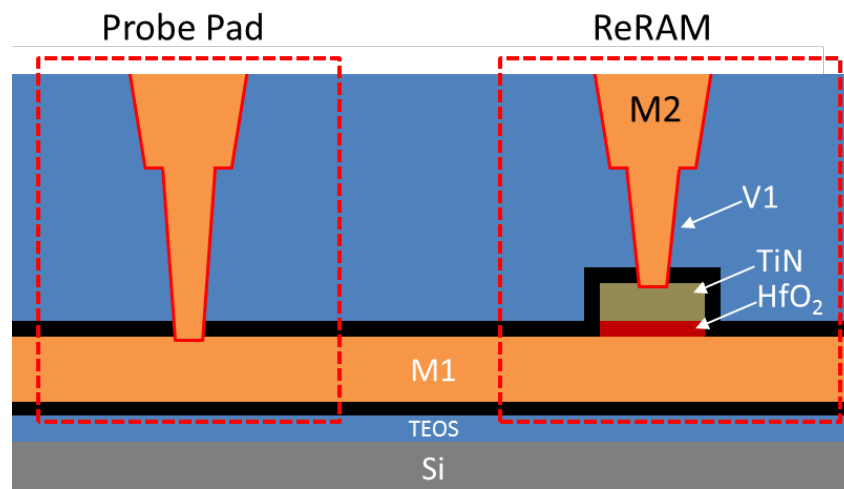


Figure 21. Schematic cross section of Raptor ReRAM fabrication.

Fabrication of the structure begins by performing a focus exposure matrix (FEM) across a wafer for each of the mask layers involved, M1, OP, V1, M2. By adjusting the optical dose (nJ) and focus (nm) one can find the correct CD values for each layer so that the printed features are as close to the as drawn layout features. The first metal layer M1 was fabricated using a standard damascene process. On a 300 mm Si wafer we deposited our M1 insulator stack of 70 nm of SiO₂ / 30 nm of SiCN / and 200 nm of SiCO by chemical vapor deposition (CVD). The SiO₂ is used to insulate the metal line from the substrate, the SiCN is a proprietary IBM material called “nBlock” which acts as an etch stop layer, and the SiCO is a 3rd generation low-k dielectric for reduced parasitic capacitances between interconnects. Post insulator deposition, a bi-layer photoresist stack (35 nm SiARC/230nm PR) was spun on and M1 lithography was performed on an ASML 1750i immersion 193 nm optical stepper. After M1 lithography, a reactive ion etch (RIE) was performed to remove the SiCO and stop on the nBlock (end point detection and selectivity of etch gasses allow for process control). RIE gas chemistries were switched to remove the nBlock. Next a 30 nm liner/seed stack of TaN/Ta/Cu was sputtered to line the M1 trench, acting as a Cu diffusion barrier, adhesion layer, and electroplating seed respectively. After liner/seed deposition, 500 nm of Cu was electroplated onto the wafer, filling the M1 trenches and producing an overburden of Cu on the wafer surface. Then chemical mechanical planarization (CMP) was performed to remove the overburden and planarize the wafer surface. Figure 22 shows a TEM cross-section of

completed M1 lines. The copper grain structure is clearly present in the M1 line as well as the high z-number Ta/TaN liner surrounding the Cu. Also present in the TEM is dishing in the low-k SiCO between interconnects. This is due to Cu CMP being a two-step process. First a low abrasive rotating pad is used in conjunction with slurry of per-oxides and silica particles to oxidize the copper overburden and mechanically remove the copper oxide respectively. The processes will naturally endpoint on the liner surface. Next a more abrasive rotating pad is used with non-oxidizing silica slurry to mechanically remove the TaN/Ta liner still present on the surface of the low-k dielectric. The liner removal is time based, after removal of the liner the abrasive pad is more selective to the brittle low-k than the Cu which results in dishing on the order of about 30 nm (Figure 22).

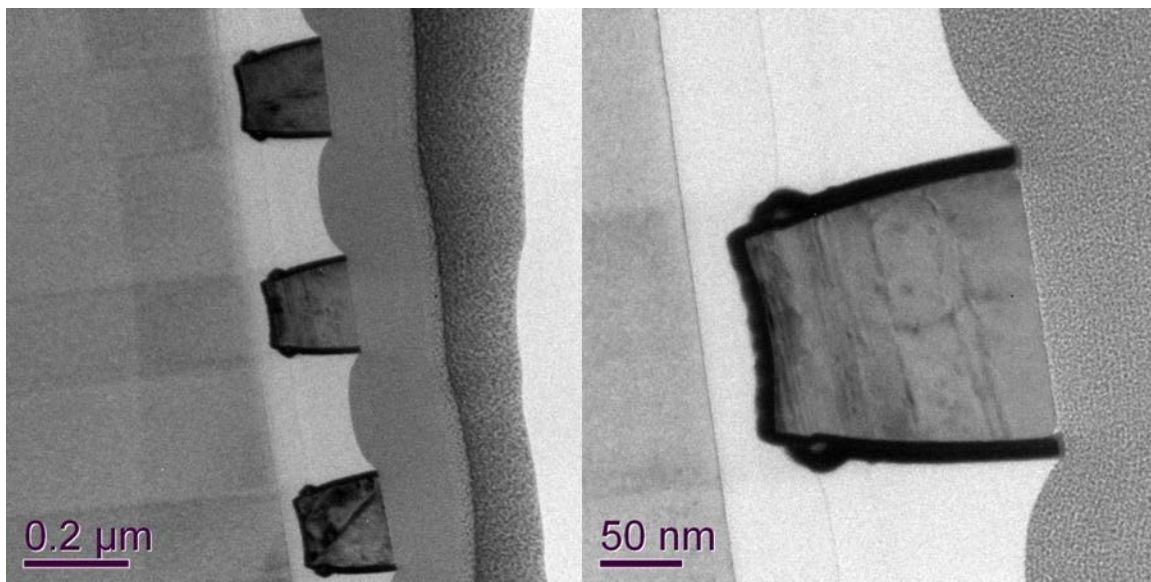


Figure 22. TEM cross-sectional micrographs of 90 nm Raptor M1 lines.

After the preceding steps, we needed to deposit our HfO_2 directly onto the Cu M1. Unfortunately HfO_2 is normally a front end of the line (FEOL) material, used as a gate dielectric. FEOL tools that deposit HfO_2 cannot have wafers that have been processed in Cu containing BEOL run through them for metal contamination reasons. Adding to this limitation, the CNSE 300 mm FAB does not have a BEOL compatible HfO_2 tool. Because of this, we have collaborated with Canon-Anelva (Japan), to deposit 15 nm of HfO_2 on our M1 wafers by reactive sputtering. After HfO_2 deposition by Canon-Anelva the wafers were shipped back to the CNSE fab and underwent several back side wet cleans to remove contamination / particulate until the wafers passed TXRF (usually 2 passes). After decontamination, 50 nm of TiN was deposited to act as an electrode and etch hard mask. Using the OP mask layer we then patterned and RIE etched the TiN. Then using the TiN OP islands as a hard mask, a dilute HF wet etch (100:1 for 4 min) was used to remove the remaining field HfO_2 , leaving our device pillar of 15 nm HfO_2 / 50 nm of TiN. Figure 23 shows a top-down SEM micrograph of the 12 x 12 crossbar structure post HfO_2 dilute Hf etch. The round 200 nm pads atop M1 lines are the features defined in the OP mask level defining the active device area.

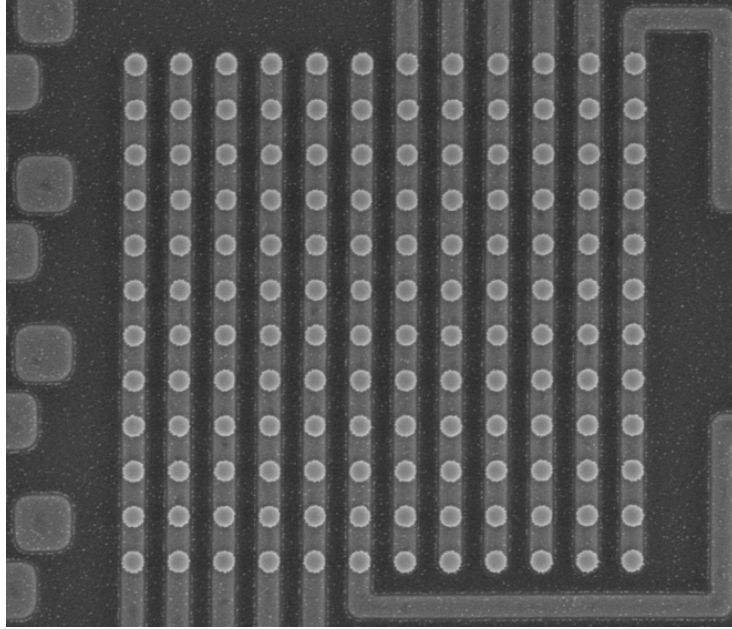


Figure 23. Top-down SEM of 12 x 12 crossbar post HF dip.

A 30 nm layer of nBlock was deposited by CVD, sealing the wafer and device surface. Next a 500 nm layer of SiCO was deposited and planarized by CMP for the V1/M2 insulator. V1 and M2 were fabricated using a dual damascene flow, in which the entire contact and line were plated together and polished as one entity. Dual damascene starts with V1 lithography and RIE etch. The RIE etch in the V1 process is of particular importance. Recalling the schematic cross-section in Figure 21, the V1 contact needs to land differentially on both the M1 Cu surface and the top of the TiN device contact. The differential etch was accomplished with a RIE chemistry (C_4F_8) that is 10:1 selective of SiCO to nBlock (SiCN), so as the etch hits the top most surface of the nBlock above the TiN OP pad (Figure 24 right) it could still etch the remaining 65 nm of SiCO in the contact pad area (Figure 24 left) while only etching ~6.5 nm into the nBlock above the TiN. After the differential V1 etch an organic planarization layer (OPL) was spun onto the wafer, filling the etch holes from V1 step. The OPL layer was then a platform for the M2 photoresist stack. Next, M2 lithography was performed, with RIE creating the trench of the M2 line connected to the V1 contact within the same insulator. The OPL layer was removed by oxygen plasma and a short RIE was used to open the remaining nBlock at the bottom of the V1 contact. Then a dilute HF clean was used to remove any etch residue and to clean the surface

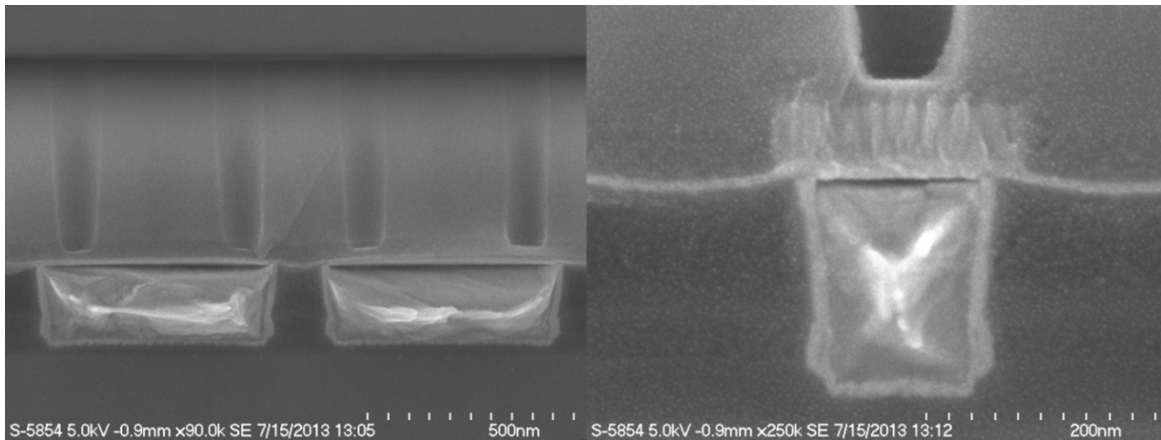


Figure 24. SEM cross-sections from pad (left) and device (right) areas, post V1 RIE.

of the Cu and TiN, of the Contact pad and TE respectively. After these steps, the process repeated the same liner/seed, electroplate, and CMP process flow from M1 (above), completing the BEOL resistive memory process. The completed device structure was imaged using a FIB-SEM dual-beam for site specific cross-sectioning. Figure 25 (left) shows several 100 nm V1 devices from a 12 x 12 crossbar structure, with M1 running horizontally and V1/M2 present in cross-section. The TiN TE with HfO₂ pad appears to be in good condition with no undercuts or delamination from the dilute HF wet etches (Figure 25 right). Lastly, **Figure 25** (right) shows good contact between the V1 and the TiN pad with no obvious nBlock or remaining SiCO, creating a strong electrical contact.

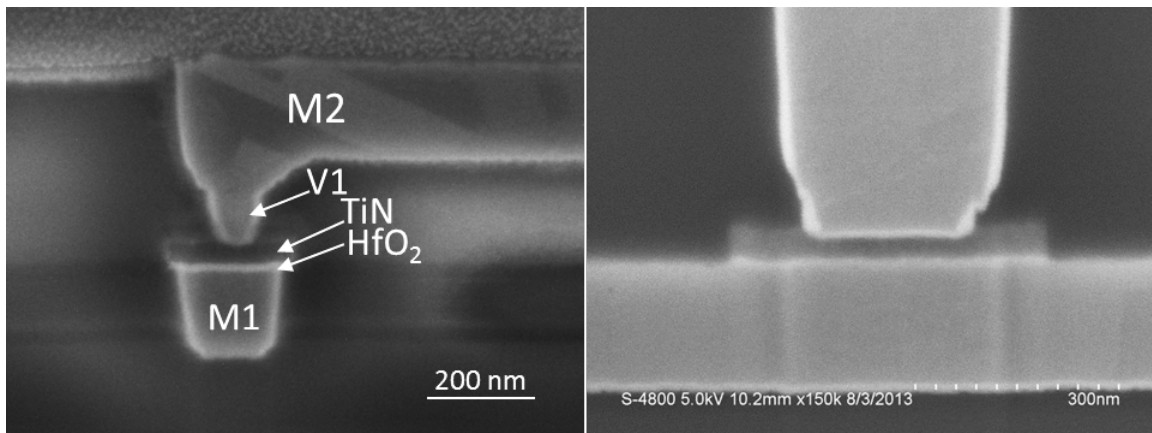


Figure 25. (Left) A FIB/SEM cross-section of a 100 x 100 nm 1R device. (Right) A higher magnification cross-section of a 200 x 200 nm 1R Device.

4.5 Reliability Studies, Device Performance and Power

Measurements were performed on single 1R cells and 12x12 crossbar arrays in a 1T1R configuration. An external transistor connected to the passive electrode was used to control the current during the forming and subsequent set operations. A yield of 100% was achieved with the 1R cells as well as the crossbar arrays and initial measurements of 1R elements showed good performance regarding endurance, on/off ratio and resistance values. Figure 26 shows the LRS,

HRS and on/off ratio of an example ReRAM for >1000 cycles. The 250x250 nm² ReRAM cell formed at 5.88 V while the saturation current of the transistor was set to 250 μ A. A periodic spiking was observed around every 60 cycles in this 1R device. This behavior can be seen as well for the crossbar array ReRAM cells (Figure 32). The phenomenon has yet to be analyzed in detail, however, it is believed to be a periodic malfunction or anomaly of the semiconductor analyzer, not the memristor devices themselves. The bypass connection at the drain of the transistor (see Figure 27b) for the reset operation must be kept at 0 A possibly causing this periodic spiking.

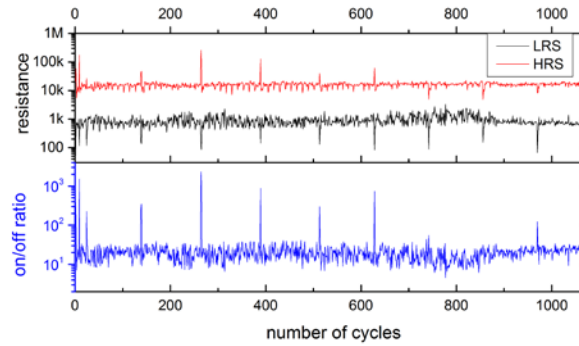


Figure 26. On/off resistance ratio, LRS and HRS is shown for 1100 cycles for a 250x250 nm² 1R (1 ReRAM) cell in an external 1T1R configuration. An N-MOSFET has been used to control the current during the set operation.

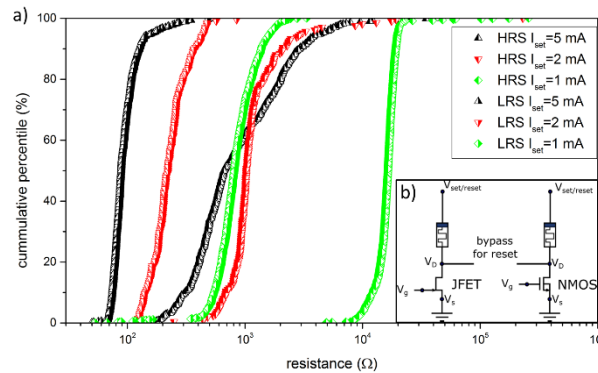


Figure 27. Cumulative percentile of LRS and HRS vs. resistance is shown for 1R elements in a 1T1R configuration for three different set currents ranging from 1 mA to 5 mA. The 1R ReRAM cells have a size of 100x100 nm².

The average on/off ratio was 27.5 and a discrete memory window throughout all cycles was achieved between the LRS and HRS without overlapping resistive states. This is important for memory applications to prevent a failure bit. The low threshold voltages with average set/reset values of 0.781/-0.54 V never exceeded the supply voltage of our CMOS design, further supporting the feasibility of an integrated ReRAM/CMOS system. The effect of changing current during the set operation has been studied for several ReRAM cell sizes and an example is shown in Figure 27 for a cell size of 250x250 nm². The cumulative percentile is plotted versus the resistance for three different set current ranging from 1 to 5 mA. It was possible to change the LRS and HRS over one order of magnitude possibly enabling multibit operations for ReRAM storage technologies.

A more comprehensive analysis with similar results was performed with the crossbar arrays regarding their dependence on the set current. The transistor was changed to a JFET, reducing parasitic capacitance, which results in a better control of the LRS during the forming and set operations. The forming current was fixed to 50 μA , which is the lowest current with which the ReRAM's operated with 100% yield. The set current was increased from 70 up to 1200 μA . A tendency towards increasing set voltages and decreasing reset voltages was observed while increasing the set current (Figure 28). The larger set current causes a thicker filament decreasing the resistance for the subsequent reset operation. The increased power dissipation within the filament (due to a higher reset current) causes an increase in joule heating. The increased temperature during the reset likely causes a larger gap between the conductive filament and the electrode and subsequently increases the voltage necessary to achieve an electric field at which the set operation occurs.

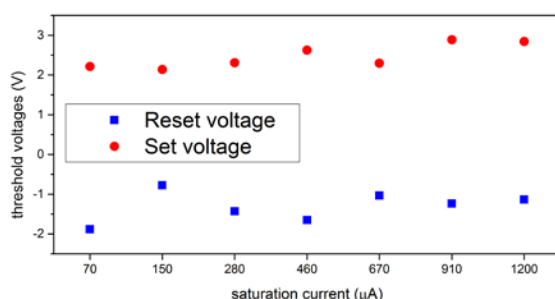


Figure 28. Threshold voltages (reset and set voltages) are shown for seven different saturation current (compliance current) levels. The saturation current was set by changing the gate voltage of an external transistor. One device was characterized with a different saturation current and cycled at least 100 times. Median values were selected to negate effect of the periodic spiking of the semiconductor analyzer.

Figure 29 shows the HRS, LRS and on/off ratio for these seven different saturation (compliance) current values. It can be observed that the on/off ratio is progressively increasing while the LRS reduces and the HRS increases. The cumulative percentile versus the resistance plot in Figure 30 shows four example saturation current values (70, 150, 280 and 1200 μA). The plot reveals that for the two lowest set currents, good control over the resistive states of the ReRAM was achieved. If the set current increases, the HRS becomes more uncertain and unstable [28]. A change in resistance over two orders of magnitude was achieved by increasing the saturation current around 15-fold, improving the previously observed results for 1R elements. The high on/off ratio comes with major disadvantages, however, such as overlapping low and high resistive states, a reduced reliability and endurance, making this operation window unfeasible for memory applications. This observation is shown for the device with a set current of 910 μA (see **Figure 29**). The linear plot of the set/reset current versus voltage illustrates a very unstable operation window with a large deviation of the set/reset voltage as well as LRS and HRS. The inset of Figure 8 shows the log plot of 5 set/reset operations and reveals the large memory window of up to 100k. A more detailed look at the low set current operation (70 μA) in Figure 32 reveals unstable operation for the first 40 cycles, caused by the forming operations at which this filament size cannot be controlled properly. This is a result of an increased forming voltage resulting in a current overshoot [25]. Even though the ReRAM must handle this immense stress, the cell is able to adjust to the low set current and

goes beyond the well-defined HRS and LRS. This transition can be seen as well in Figure 30 (black curves) where around 25% of the resistance values strongly deviate from the median value.

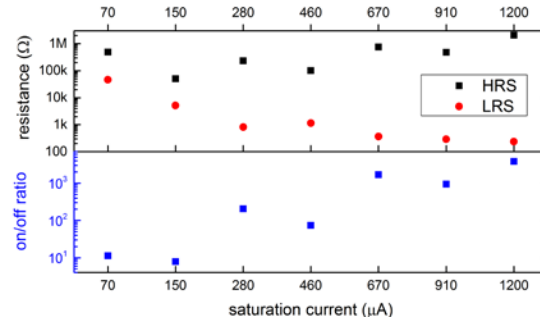


Figure 29. LRS, HRS and on/off ratio is shown for seven different saturation currents. The saturation current values were set by changing the gate voltage of a JFET. One device was characterized with a different saturation current and cycled at least 100 times. Median values were selected to cancel out the effect of the periodic spiking of the semiconductor analyzer.

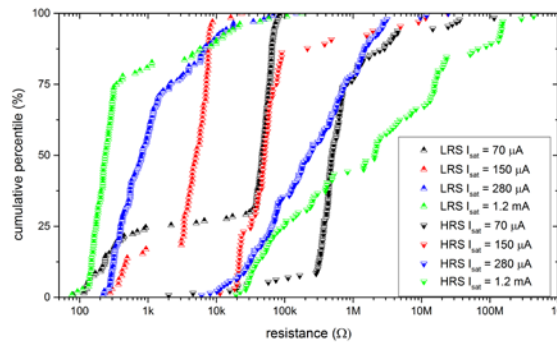


Figure 30. Cumulative percentile of LRS and HRS vs. resistance is shown for ReRAM cells in a crossbar array for four different set currents ranging from 70 μA to 1.2 mA. The ReRAM cells have a size of 100x100 nm².

The I-V characteristics for the cycles between two spikes is shown in Figure 33. These data reveal an excellent predetermined set/reset operation with low deviation and reset currents below 50 μA . The insets in the figure show the preceding traces during the spiking. After a normal set operation the semiconductor analyzer sweeps to its maximum voltage (10 V) where at some point after the first set a second increase in current is recognized. This is possibly caused by the aforementioned current spike through the bypass at the drain of the transistor. The ReRAM typically does not need more than two cycles to recover from the malfunction, demonstrating excellent recoverability.

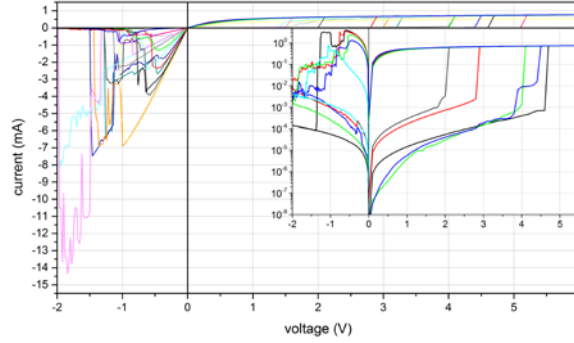


Figure 31. I-V characteristics are shown for 15 example set/reset cycles of a crossbar ReRAM cell operated in a 1T1R configuration. The saturation current of the transistor is set to 910 μA . The inset shows a subset of the 15 example traces in log scale.

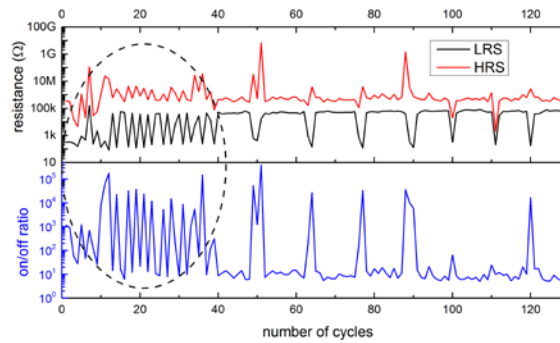


Figure 32. On/off ratio, LRS and HRS is shown for ~ 130 cycles crossbar ReRAM cell ($100 \times 100 \text{ nm}^2$) in an external 1T1R configuration. The external transistor was used to limit the current to 70 μA during the set operation.

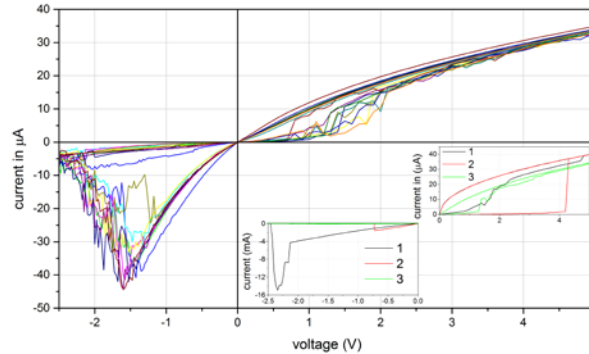


Figure 33. I-V characteristics are shown for the crossbar ReRAM cell operated in a 1T1R configuration. The saturation current of the JFET was set to 70 μA . The 10 set/reset operations show the behavior between the spikes at around 65 and 75 cycles (resistance values shown in Figure 32). The insets show the three set (right inlet) and reset (left inlet) operations prior the traces in the main graph.

4.6 Power Comparison

Power consumption in integrated circuits become more and more import with respect to many aspects of their applications. From our everyday life where the battery of the smartphone

should last as long as possible to computing centers where the power consumption is responsible for a high percentage of the operation costs. This impacts our convenience and contributes to green-house gas emission. Innovative solution have to be made to counteract this. A suggestion has been made to improve the power consumption of a security application which are typically consuming over-proportional amount of power than other systems if executed on non-optimized CMOS circuitry. By implementing a solution based on hybrid ReRAM/CMOS for the Advanced Encryption Standard (AES) we are able to considerably reduce the power consumption.

The proposed design of the XOR cell shown in Figure 34 (a) shows the initial proposed structure from Abid et al. 2009 (IEEE Transactions on Nanotechnology, 8(3): 315-321, 2009), which we modified to include pull-down resistive elements to establish a defined level for the inputs (to ultimately enable proper switching in our hybrid ReRAM/CMOS XOR implementation (Fig. 1b)

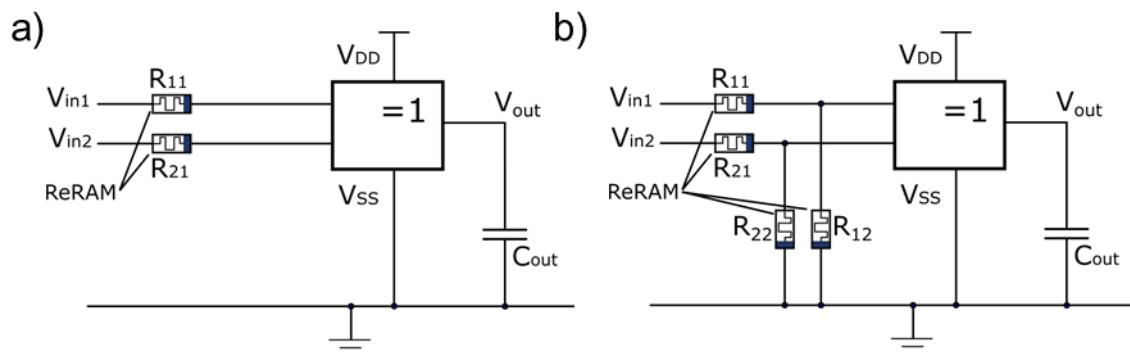


Figure 34. Hybrid ReRAM/CMOS design a) without pull-down ReRAM and b) with pull-down ReRAM.

This circuit was implemented in CNSE's 300mm fabrication facility using the IBM 65 nm 10LPe process flow. Hafnium oxide based ReRAM was implemented in the back end of the line (BEOL) portion of the process, defining ReRAM elements at M1. Top level circuit design and the implemented circuit are shown in Fig. 2.

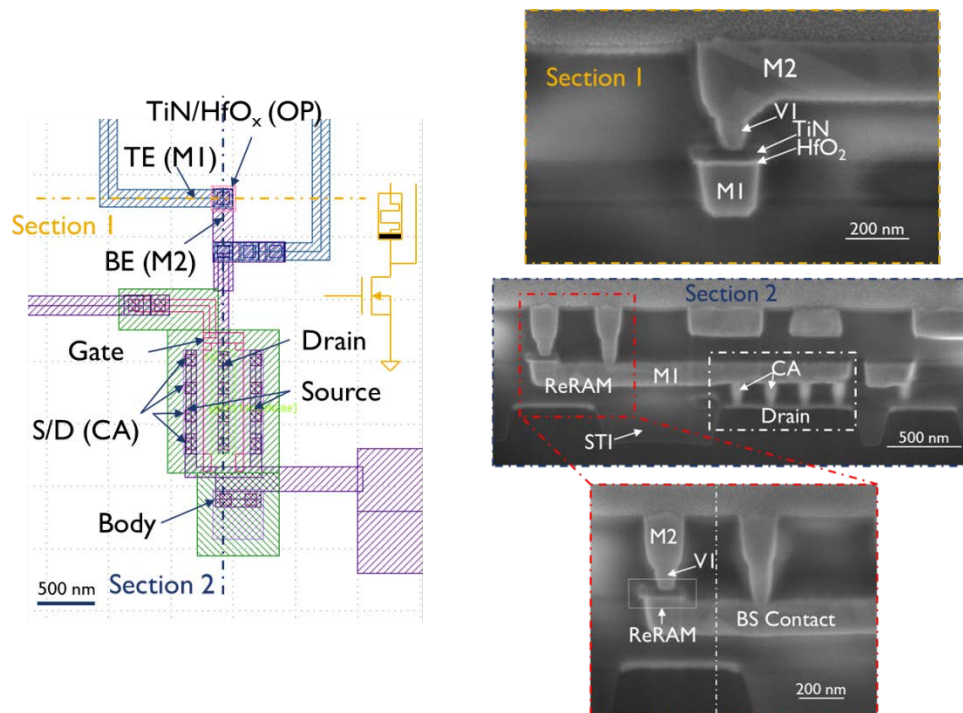


Figure 35. LRS, HRS and on/off ratio vs. number of cycles for a ReRAM operated in an external 1T1R configuration with a saturation current set to 70 μA .

We have demonstrated both binary switching of ReRAM elements fabricated in this flow, as well as control of LRS and HRS values via manipulation of the saturation current during ReRAM set/reset (Fig 3). We reliably achieve median values of LRS and HRS of 47 k Ω and 496 k Ω (Fig. 3, black triangles).

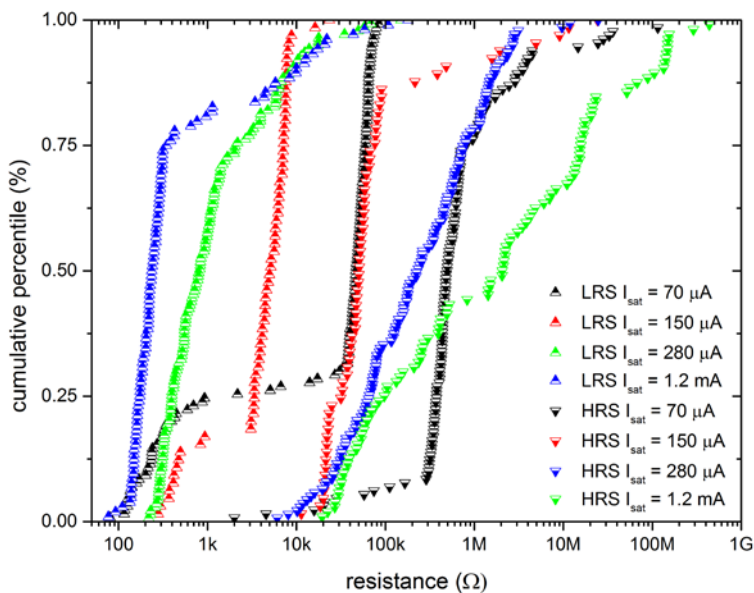


Figure 36. Cumulative percentile of LRS and HRS vs. resistance is shown for ReRAM cells in a crossbar array for four different set currents ranging from 70 μA to 1.2 mA. The ReRAM cells have a size of 100x100 nm².

With these values we can calculate the power consumption by each ReRAM input/output for the hybrid ReRAM/CMOS XOR circuit:

$$I_{C_ReRAM} = \frac{V_{DD}}{R_{HRS} + R_{LRS}} = \frac{1V}{47k\Omega + 496k\Omega} = 1.842 \mu A$$

$$P_{C_ReRAM} = I_{C_ReRAM} \cdot V_{DD} = 1.842 \mu W$$

For an optimized implementation with 120 kohm R_{on} (which was figure of merit for the original design, and which we are working to implement via engineering of the switching dielectric and dielectric/electrode interface). By improving the ReRAM R_{on} / R_{off} , we estimate a further reduction in power utilization:

$$I_{C_ReRAM} = \frac{V_{DD}}{R_{HRS} + R_{LRS}} = \frac{1V}{120k\Omega + 1.2M\Omega} = 0.758 \mu A$$

$$P_{C_ReRAM} = I_{C_ReRAM} \cdot V_{DD} = 0.758 \mu W$$

Using these power estimates and a conservative assumption that there is a 50% likelihood of the circuit in the “on / high” state, we estimate the following power consumption values for XOR and AND/XOR cells following the original design by Abid *et al.* (XOR_only MixColumn cell, and AND/XOR Subbytes cell):

Current CNSE ReRAM/CMOS implementation:

$$P_{C_XOR} = P_{C_ReRAM} \cdot \frac{1}{2} \cdot 3 = 2.763 \mu W$$

$$P_{XOR_only} = P_{C_XOR} \cdot 2 + P_{\text{OriXOR}_{only}} = 2.763 \mu W \cdot 2 + 1.5 \mu W = 7.03 \mu W$$

$$P_{AND/XOR} = P_{C_XOR} \cdot 2 + P_{\text{OriAND}_{XOR}} = 2.763 \mu W \cdot 2 + 4.5 \mu W = 10.03 \mu W$$

Optimal CNSE ReRAM/CMOS implementation:

$$P_{C_XOR} = P_{C_ReRAM} \cdot \frac{1}{2} \cdot 3 = 1.137 \mu W$$

$$P_{XOR_only} = P_{C_XOR} \cdot 2 + P_{\text{OriXOR}_{only}} = 1.137 \mu W \cdot 2 + 1.5 \mu W = 3.76 \mu W$$

$$P_{AND/XOR} = P_{C_XOR} \cdot 2 + P_{\text{OriAND}_{XOR}} = 1.137 \mu W \cdot 2 + 4.5 \mu W = 6.77 \mu W$$

A summary of the power consumption by the original theoretical implementation and the CNSE implementations follows in Table 2:

Table 2. Average power consumption of the XOR-only and AND/XOR gates implemented in CMOS and hybrid ReRAM/CMOS from original theoretical study (Abid et al., 2009) and CNSE implementations.

	Power Consumption (μ W)		Power Reduction (vs. CMOS-only)	
	XOR only	AND/XOR	XOR only	AND/XOR
CMOS-only implementation (Abid, 2009)	10.5	16.3	--	--
Theoretical Hybrid ReRAM/CMOS (Abid, 2009)	1.5	4.5	7X	3.6X
CNSE Implemented Hybrid ReRAM/CMOS (47 k Ω ReRAM LRS)	7.03	10.03	1.5X	1.6X
CNSE Optimal Hybrid ReRAM/CMOS (120 k Ω ReRAM LRS)	3.76	6.77	2.8X	2.4X

5. Conclusions

In this effort, the goal was to design, fabricate and test a reconfigurable unit cell (XOR) that could be used for AES encryption applications. The purpose of implementing a hybrid ReRAM/CMOS reconfigurable XOR cell was two-fold: 1) to save chip area / hardware in an AES hardware implementation, and 2) to reduce total power consumption versus a traditional, CMOS-only AES implementation. The goals of the effort were met, if not exceeded, as we have demonstrated a fully-integrated hybrid ReRAM/CMOS XOR unit cell and have demonstrated high switching endurance and even multi-level switching for the ReRAM component. The functionality of our reconfigurable XOR logic was demonstrated, as well as additional ReRAM implementations, including high density crossbar arrays (128 x 128) with nanoscale ReRAM nodes (100 nm x 100 nm device size). Further, the demonstrated multi-level switching capacity of our hafnium oxide based ReRAM sets the stage for follow-on efforts that can utilize multi-level memory. These include neuromorphic applications in which ReRAM elements can be used to store the effective ‘weight’ of synaptic connections between neural synapses in a hardware implementation of neurons / neural arrays. The Verilog models and SPICE based simulations that were developed under this effort will pave the way for the design of more complex circuits that integrate ReRAM with CMOS, including both reconfigurable circuits, as well as complex neuromorphic systems. Further, the functionality of the hybrid devices, especially the reconfigurable XOR could pave the way for low power, reduced area AES hardware implementations, as was the original goal of this work.

6. Presentations, Publications and Patent Applications Resulting from this Project

Peer-Reviewed Journal Articles

1. K. Beckmann, H. Manem, N.C. Cady, "A Novel Time-Delay PUF Design Utilizing Integrated Nanoscale ReRAM Devices," *submitted to IEEE Transactions on Emerging Topics in Computing*, September 2015.
2. B.D. Briggs, S.M. Bishop, K.D. Leedy, N.C. Cady. Characterization of hafnium oxide resistive memory layers deposited on copper by atomic layer deposition. (2014) *Thin Solid Films*. 562: 519-524.
3. S.M. Bishop, B.D. Briggs, P.Z. Rice, J.O. Capulong, H. Bakhru, N.C. Cady. Ion implantation synthesis and conduction of tantalum oxide resistive memory layers. (2013) *Journal of Vacuum Science & Technology B*. 31(1): 012203.
4. P.Z. Rice, B.D. Briggs, S.M. Bishop, N.C. Cady. Development of a silicon oxide based resistive memory device using a spin-on hydrogen silsesquioxane precursor. (2012) *Journal of Materials Research*. 27: 3110-3116.
5. S.M. Bishop, H. Bakhru, J.O. Capulong, N.C. Cady. Influence of the SET current on the resistive switching properties of tantalum oxide created by oxygen implantation. (2012) *Applied Physics Letters*. 100, 142111.
6. N.R. McDonald, S.M. Bishop, B.D. Briggs, J.E. Van Nostrand, N.C. Cady. Influence of the plasma oxidation power on the switching properties of Al/Cu_xO/Cu memristive devices. (2012) *Solid-State Electronics*. 78: 46-50.
7. S.M. Bishop, H. Bakhru, S.W. Novak, B.D. Briggs, R.J. Matyi, and N.C. Cady. Ion Implantation Synthesized Copper Oxide-based Resistive Memory Devices. (2011) *Applied Physics Letters*. 99, 202102.
8. J.E. Van Nostrand, R. Cortez, Z.P. Rice, N.C. Cady, and M. Bergkvist. Morphology, Microstructure and Transport Properties of ZnO Decorated SiO₂ Nanoparticles. (2010) *Nanotechnology*. 21 415602.

Patents

1. "Hardware based random number generator." U.S. Patent 8,680,906 B1, March 25, 2014.
2. "Ion Bombardment Synthesis of Transition Metal Oxide-Based Memory Devices." U.S. Patent Application, Filed August 23, 2011: US Serial No. 61/526537.

Peer-Reviewed Conference Proceedings Papers

1. G. Chakma, H. N. Hughes, M. E. Dean, G. S. Rose, H. Manem, K. Beckmann and N. C. Cady "Device and Circuit Considerations for a Memristive Dynamic Adaptive Neural Network Array," *submitted to IEEE Symposium on Circuits and Systems (ISCAS)*, 2016.

2. M. Uddin, A. R. Wyer, G. S. Rose , K. Beckmann, H. Manem, Z. Alamgir and N. C. Cady "Reliability Analysis of a Crossbar PUF Built from Hafnium-Oxide Memristive Devices," submitted to *IEEE Symposium on Circuits and Systems (ISCAS)*, 2016.
3. H. Manem, K. Beckmann, M. Xu, R. Carroll, R. Geer and N. C. Cady, "An Extendable Multi-Purpose 3D Neuromorphic Fabric using Nanoscale Memristors," *IEEE Symposium on Computational Intelligence for Security and Defense Applications (CISDA)*, May 2015.
4. N. C. Cady, K. Beckmann, H. Manem, M. E. Dean, G. S. Rose, and J. Van Nostrand, "Towards Memristive Dynamic Adaptive Neural Network Arrays," invited abstract submitted to *41st Annual GOMACTech Conference*.
5. K. Beckmann, J.S. Holt, J.O. Capulong, Z. Alamgir, S. Lombardo, J.E. Van Nostrand, N.C. Cady. Endurance and reliability of hybrid CMOS/ReRAM for data storage and encryption applications. *GOMACTEC Conference, March 2014, St. Louis, MO*.
6. K. Beckmann, J. Holt, J.O. Capulong, S. Lombardo, J.E. Van Nostrand, N.C. Cady. Reliability of fully-integrated nanoscale ReRAM/CMOS combinations as a function of on-wafer current control. (2014) *IEEE International Integrated Reliability Workshop 2014*.
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13. B.D. Briggs, S.M. Bishop, K.D. Leedy, B. Butcher, R. L. Moore, S. W. Novak, and N.C. Cady. Influence of Copper on the Switching Properties of Hafnium Oxide-Based Resistive Memory. (2011) *Proceedings of the Materials Research Society*, San Francisco, CA.

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8. List of Acronyms

RRAM:	Resistive random access memory
ReRAM:	Resistive random access memory
RMD:	Resistive memory device
TE:	Top electrode
BE:	Bottom electrode
HRS:	High resistance state
LRS:	Low resistance state
XPS:	X-ray photoelectron spectroscopy
XRD:	X-ray diffraction
TEM:	Transmission electron microscopy
CMOS:	Complimentary Metal-Oxide-Silicon
AES:	Advanced Encryption Standard